SAMPLING OSCILLOSCOPE CIRCUITS

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CIRCUIT CONCEPTS

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PREFACE

This information is primarily for people who want to understand how sampling oscilloscopes work. It is particularly slanted toward instrumentation engineers, oscilloscope calibration men and owners and users who want best performance from their instruments.

Only key circuits and concepts unique to Tektronix sampling oscilloscopes are covered. Circuits common to sampling and conventional scopes are discussed in other books in this series. A list of those books will be found facing the inside back cover.

Probably the most imaginative sampling-circuit concepts are the ones that pertain to the manner in which the more basic circuits are related to each other. Understanding these broader *relatedness* concepts is normally tougher than perceiving ingenious circuit details. The best way we know to explain the relatedness concepts is by use of block diagrams and waveform time-relationship diagrams. Basic circuit functions are categorized, named and grouped into blocks showing their relationships. No one is expected to deduce the concepts from the diagrams alone. Each function is explained in detail in Chapter 2.

All the *circuits* discussed in Chapters 3, 4, 5 and 6 are good examples of the basic circuit *functions* described in Chapter 2. The circuit diagrams in this book are reproduced from actual diagrams that appear in the instruction manuals for various Tektronix sampling instruments in production in mid 1969. They do not include the 7S11 Sampler or 7T11 Sampling Time Base Unit announced in August 1969. Because the reproductions are greatly reduced in size, some details such as connector pin numbers and circuit symbol numbers are deleted for sake of clarity and simplicity. Sections of the diagrams have been shaded to correspond to the blocks in the block diagrams. We hope this helps you relate the details of how a circuit operates to its *purpose* for being there.

We have not extracted any section of a circuit diagram to place it closer to the text that describes that section even though we know it would make the job of switching your eyes between text and diagram easier. If you remember that the text always pertains to the closest diagram on an earlier page, relating the two will be simpler.

The diagrams were selected so that all of what might be called *key* sampling circuits (in mid 1969) could be described here. For sake of completeness, however, the circuits on each diagram that are not what might be called key circuits are also described. A list of circuits similar to the ones described appears as part of the index.

1

INTRODUCTION TO SAMPLING PRINCIPLES

Sampling scopes have been commercially available since about 1959. Their primary advantage is their ability to respond to small fast-changing signal voltages better than conventional scopes.

strobe pulses

The most fundamental sampling principle is analogous to the principle of optical stroboscopes. A stroboscope generates very brief flashes of light which, when properly timed, can make rapidly moving things appear to be at rest or occurring in slow motion. Sampling scopes graphically depict fast-changing voltages as if the changes were occurring slowly. Instead of generating flashes of light however, sampling scopes generate very brief electrical pulses. These pulses allow us to "look" at a repetitive signal one point and one cycle at a time and depict the signal character graphically but slowly over a period of many cycles. Until recently, the brevity of the pulses determined the shortness of risetime. For example, pulses 350 ps in duration are used in sampling scopes having a risetime of 350 ps. This risetime is comparable to a bandwidth of 1 GHz -- one-billion cycles per second! These pulses are called strobe pulses because of their similarity in function to the flashes of light from a stroboscope.

useful features

Although the faster response of sampling scopes is their principle attraction, they have three other features that make them especially useful. First, the process of taking and storing samples of a repetitive signal is such that sampling scopes are almost completely free from display aberrations caused by overscanning the screen. Secondly, large, permanent, paper-chart recordings can be made of a displayed signal directly from *X* and *Y* coordinate output signals. And third, the process of sampling lends itself to digitizing time measurements directly, even extremely short intervals of time, and to making digital measurements of the voltage difference between two points on a very fast-changing signal. Sampling scopes were forerunners of digital-readout scopes.

The principle of sampling electrical signals was known before the turn of the century. In 1880 Joubert devised a way of sampling a power-generator waveform with a pen and ink recorder. This was well

before the days of even simple oscilloscopes. In the 1950's when transistors became available, the work of J. G. McQueen, R. Sugarman, R. Carlson and others paved the way to practical commercial sampling oscilloscopes. Even the very first commercial sampling scopes had much shorter risetimes than any conventional scope which used a vertical-deflection amplifier.

using semiconductor devices

The fundamental reason why sampling scopes can respond to faster-changing signal voltages than conventional scopes is that with certain semiconductor devices we can generate much narrower pulses than we can amplify. With vacuum tubes this was not so.

Besides generating narrow pulses we must cause them to occur at the right moments. Tektronix presently uses four methods of timing strobe pulses. All four result in a CRT display comprised of a series of dots -- one dot per sample. When the dots occur at a high repetition rate and are closely spaced they may give the appearance of a continuous trace.

sequential and random sampling

Two of the names given to the timing methods are based on the appearance of a trace for that mode. The first and most common mode is called sequential sampling. With sequential sampling the display is comprised of a very orderly series of equally spaced dots resulting from equally spaced steps of the CRT beam. The second mode is called random sampling. With random sampling successive dots may occur at what appears to be random horizontal positions while plotting the graph.

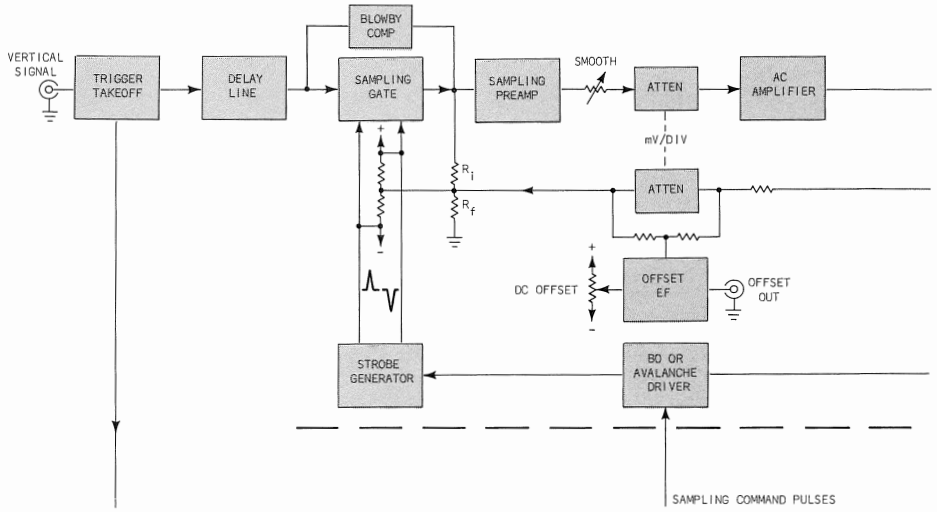
real-time sampling

The other two timing methods are used in the mode called real-time sampling. With real-time sampling we do not attempt to depict fast changes in slow motion. In fact, that system is not one of depicting fast changes at all, but rather is a way of extending the use of sampling scopes to look at very *slow* voltage changes. With real-time sampling, unlike sequential sampling and random sampling, the horizontal time scale of the scope is equal to the actual time the beam takes to traverse horizontally the divisions on the screen.

With sequential sampling and random sampling, the time required to make one complete sweep (scan) of the beam across the screen is vastly longer than the time represented by the full horizontal scale. That tells us the time per division of the scale is much less than the horizontal beam velocity. With either of the modes, the vertical and horizontal (*X* and *Y*) coordinate relationships are precisely maintained to produce a coherent, graphic, scope display. How all these good things are made to happen will be the subject for the following pages!

2

BASIC CIRCUIT FUNCTIONS AND RELATIONSHIPS


VERTICAL SIGNAL
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BLOWBY COMP
SAMPLING GATE
SAMPLING PREAMP
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AC AMPLIFIER
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DC OFFSET
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OFFSET OUT
STROBE GENERATOR
BO OR AVALANCHE DRIVER
SAMPLING COMMAND PULSES

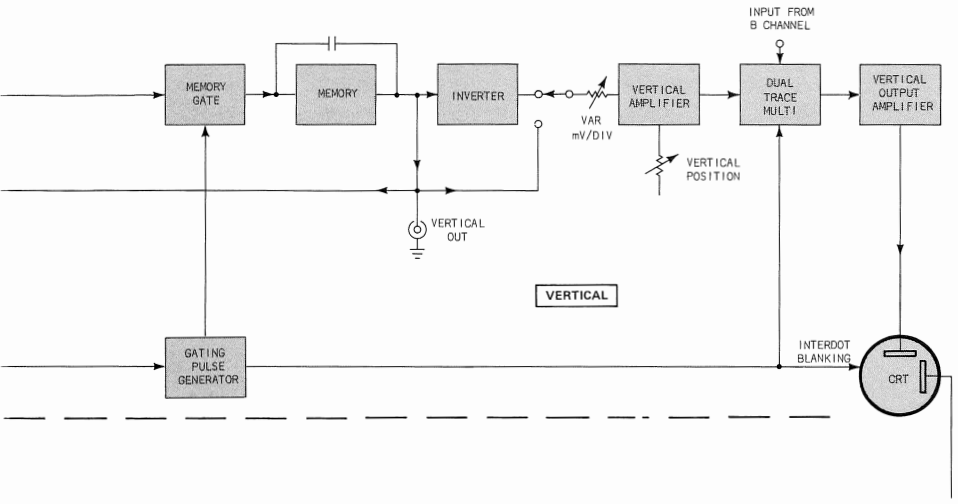


Fig. 2-1. Basic block diagram of vertical deflection section.

SAMPLING, AMPLIFYING, HOLDING, FEEDING BACK

The block diagram in Fig. 2-1 represents the function to be discussed.

delay line

Notice that a delay line is shown between the trigger takeoff and the sampling gate. Sampling instruments having a shorter risetime than about 350 picoseconds do not have delay lines. But delay lines are not always used, even when the risetime is 350 picoseconds or longer. This delay line is a specially constructed, 50-ohm coaxial cable about thirty to fifty feet long having a delay of about 45 to 75 ns. A delay line this long, having dimensions small enough so it can be wound up and placed inside of a sampling scope, will degrade the response to fast-step signals. In particular, the top corner of a rising-step signal (or the bottom corner of a falling-step signal) will be rounded. See Fig. 2-2. When we use such a delay line, therefore, we usually have a passive compensation circuit at the end of the delay line that provides a correction for the degradation of waveshape introduced by the delay line. The end of the delay line is terminated in this network.

sampling gate

The sampling gate is connected at the end of the network and at this point blocks further passage of the input signal nearly all the time. The purpose of the sampling gate is to block the signal except during the very brief moments when the signal voltage is allowed to go through the gate and into the sampling preamplifier.

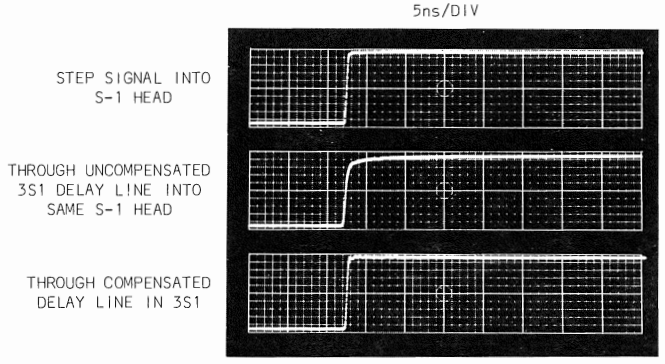


Fig. 2-2. Delay-line dribble-up. 70-ps step signal from Type 284 displayed on 561B (projected graticule).

Typically, Tektronix sampling instruments do not sample any signal more often than 100,000 times a second, regardless of the signal frequency. Trigger countdown is always to 100 kHz or less. Sampling 100,000 times a second, when the sampling gate is opened for only 350 picoseconds for each sample, provides a sampling duty factor of only about one part in 30,000.

back-bias voltage

The sampling gate consists of two to six very fast low-storage diodes. These diodes are arranged to have a back-bias voltage applied across them at all times except when we wish the signal energy to pass through. The back-bias voltage is usually derived by tapping a couple of points in a resistive DC-voltage divider. In the block diagram shown, we can see that the two inputs to the bottom part of the sampling gate block have two different voltages applied; one negative and one positive with respect to ground. The center-tap voltage is normally within ±1 volt of ground. The back-bias voltage must be high enough to be greater than the peak amplitude of the signal being applied to the input of the sampling gate, or the signal itself will cause one or more of the diodes to conduct, passing the signal at the wrong moments. The sampling-gate diodes are only supposed to conduct at the moments when we want samples to be taken. The same two lines coming into the sampling gate that bring in the back-bias voltage also bring strobe pulses from the strobe-generator block.

strobe generator

Strobe generators usually employ snap-off diodes (also called step-recovery diodes) to generate very narrow pulses. The pulses are invariably applied push-pull with the right polarity to overcome the back-bias on the sampling-gate diodes. In this block diagram the strobe generator is being driven by either a blocking oscillator or a transistor operated in the fast-switching avalanche mode. In turn this circuit is driven by the sampling-command pulses that originate in the horizontal-deflection section. Everytime a sampling-command pulse is generated, a pair of strobe pulses is delivered to the sampling gate. The strobe pulses admit the signal to the preamplifier but for only a very brief time. That time is normally equal to the duration of the strobe pulses themselves.

sampling preamplifier

Let's consider what happens just before and during the time when the sampling gate allows the signal to come through into the sampling preamplifier. A pair of strobe pulses are generated and applied to the sampling gate, overcoming the back-bias on the sampling-gate diodes and admitting the signal through the sampling gate into the sampling preamplifier. There is invariably a small amount of stray capacitance to ground at the input to the preamplifier, and this capacitance gets partially charged to the voltage which exists on the input side of the sampling gate. The capacitance would get fully charged if the strobe pulses were wider. When the sampling gate stops conducting, a small voltage will have been developed across this capacitance and will last for a relatively long time because it has a high-resistance path through which to discharge. The waveform at the input to the sampling preamplifier is a step signal having a transition time about equal to the risetime of the sampling scope.

The resistor R_i shown in the path to ground at the input of the sampling preamplifier has a relatively high resistance compared to the input impedance of the sampling gate. When driven by the input signal, the stray input capacitance can charge or discharge rapidly compared to the time taken for discharge through resistor R_i. We may see that a voltage step has been applied to the sampling preamplifier which is captured as a charge on the input capacitance. The sampling preamplifier responds to this step as fast as it can and its output is applied through a couple of attenuators, one of which is called a smoothing control, amplified further through a stage usually called an AC-amplifier stage, and then is applied to a gate at the input to the memory.

memory gate

The memory gate is very similar in some respects to the sampling gate, but is operated for a much longer period of time. Typically, the memory gate will pass the amplified signal for about one-third *microsecond* each time there is a sampling-command pulse. Compared to a third of a nanosecond or less when the sampling gate is passing the input signal, we have approximately a 1000-to-1 ratio. Notice, however, that the memory gate and the sampling gate are both turned on by the sampling-command pulses that come from the horizontal-deflection section. Not evident in the block diagram

is the fact that the memory-gating pulses, although starting simultaneously with the strobe pulses, are not turned off until much later. This tells us that a small step voltage, applied to the input of the sampling preamplifier, can be amplified for a large fraction of a microsecond while being applied through the memory gate to the memory, before the memory gate interrupts the amplified step-signal.

memory

The memory is a DC-coupled inverting amplifier with the output fed back to the input through a memory capacitor. Whenever the memory gate is open and not allowing a signal to go through, the gate disconnects the input to the memory capacitor providing only a very high impedance to ground at the input side. That tells us that whatever voltage is stored in the memory capacitor can remain essentially constant until another sample is taken. The output voltage of the memory amplifier goes to the vertical amplifier, producing vertical deflection. Each change in voltage at the output of the memory is a step change, a step proportional in amplitude to a step at the input to the preamplifier.

The amplifier stages which follow the memory output are very similar to the amplifiers in conventional oscilloscopes. There is nothing very unique about these stages.

feedback attenuator

The output of the memory amplifier also goes back to the sampling-preamplifier input, through an attenuator. The attenuator circuit consists of the resistor connected directly to the output of the memory, plus a selectable resistor connected to the first resistor, then to the resistor to ground, R_f. The amount of voltage which is developed across resistor R_f is the voltage which is applied to the sampling preamplifier from the memory output. The voltage at the memory output is, therefore, attenuated a certain amount before being reapplied back to the sampling-preamplifier input. The voltage existing across this resistor is partly determined by the DC-offset setting. For the time being we will consider the voltage across this resistor to be determined only by the output of the memory. That is, we will assume the DC-offset voltage is set to zero volts.

Nothing in the block diagram indicates what the polarity or phase of the memory-output voltage may be compared to the signal voltage sampled. It is important to know that a step in one direction at the sampling-preamplifier input invariably produces an amplified step in the *same* direction at the memory output. From this we can see that *the feedback is always in phase with the input step.* Nonetheless, the feedback from the memory output to the sampling-preamplifier input is part of a null-seeking servo loop. We call it a *sampling loop.* With each sample, the memory output repeatedly attempts to reduce the voltage existing between the input and the output of the sampling gate to zero. If the input voltage is the same each time it is sampled, the feedback matches it, reducing the difference and the size of the steps to practically zero.

sampling loop

The sampling loop is comprised of (1) the sampling gate, (2) all the amplifier and attenuator stages up to the output of the memory, and (3) the feedback path from the output of the memory to the input of the preamplifier. The input to the sampling gate is the input to the sampling loop. The percentage of signal voltage transferred across the sampling gate when the gate conducts is referred to as *sampling efficiency.* Sampling efficiency is primarily a function of strobe width, source impedance and preamplifier input capacitance. It is usually less than 25% for risetimes less than 350 picoseconds. If we have a signal level at the sampling-gate input which, at the moment the signal is first sampled, differs from the level at the output by one volt and we have a sampling efficiency of 25%, a 1/4-volt step will appear at the input to the sampling-preamplifier stage. The risetime of that step? Very nearly the same as the interval the gate was conducting.

sampling efficiency

The amplification of the step signal through the sampling preamplifier, the AC amplifier, and the memory amplifier, comprises what we call *forward gain.* How much the signal at the output of a memory is attenuated before it is fed back and reapplied to the input of the sampling-preamplifier stage is called *feedback attenuation.* The product of sampling efficiency, forward gain and feedback attenuation (with feedback attenuation expressed as gain) is what we call sampling-loop gain. Sampling-loop gain should normally be close to unity (1).

forward gain

feedback attenuation

sampling-loop gain

Let's consider what happens when the right conditions prevail to give us a loop gain of 1. First of all, let us assume that the voltage of the signal when first sampled is 10 mV above ground. The voltage applied to the sampling-preamplifier input will therefore be 2.5 mV after the first strobe pulse causes the sampling gate to conduct. If we have a forward gain of 400, the memory output will be +1 volt (400 x 0.0025). If the output of the memory is attenuated by a factor of 100 before being reapplied to the sampling-preamplifier input, then +10 mV will be fed back to this input. Ten millivolts, remember, was the level of the signal at the moment when sampled. Under these conditions we will have unity loop gain, a loop gain of one. That is because a sampling efficiency of 0.25 multiplied by a forward gain of 400 multiplied by a feedback attenuation of 1/100 equals 1.

When loop gain is 1, the voltage fed back and applied to the sampling preamplifier between strobes will be precisely the same voltage as applied to the sampling-gate input at the moment the signal was last sampled. This is usually the ideal set of circumstances.

DC offset

Now let's consider how the DC-offset control works. The primary purpose of this control is to allow us to sample and display small voltage changes on top of large DC levels at high sensitivities. We can typically offset a DC level that is, in effect, as much as 500-divisions off-screen vertically. For example, we can offset an input level of +1 volt at a sensitivity of 2 mV/div, a ratio of 500 to 1. When we say we are offsetting an input level of +1 volt at 2 mV/div, it means we set things so that a zero-volt signal level would be about 500 divisions off-screen and a 1-volt level is near center screen. We can regard the internally applied voltage as bucking the externally applied voltage. But at first it will seem strange that both voltages will have the same polarity.

When we internally apply a DC-offset voltage, we tend to develop that voltage across R_f in the feedback path by applying a specific constant current through R_f. When no signal is applied to be sampled, the voltage sampled is always zero volts. Let us assume no signal is applied. If we apply a DC-offset voltage of +1 volt across R_f, that voltage will appear at the amplifier input across the input capacitance. Then, when we first sample the input voltage (zero volts),

the capacitor partially discharges and the step change is amplified, transferred to the memory, held and fed back. The size of the step will be the same as if zero volts had initially existed across the capacitor and a 1-volt *signal* had been applied. The direction of the step will be down, as if the applied signal was negative in polarity, because the 1-volt level will *diminish* when the sampling gate conducts. The resulting step-voltage output from the memory would therefore be negative in polarity and would be larger than 1 volt in amplitude because of forward gain. The actual amplitude would depend on the forward gain and on the sampling efficiency. But if we assume that we have a loop gain of 1, the fed back portion, the portion existing across R_f, should be *equal to that which existed across the sampling gate when the sample was taken*. In other words, the feedback tries to place minus 1 volt across the same resistor that we had deliberately placed plus 1 volt across with the DC-offset control. The net effect is that essentially zero volts will be developed across the resistor R_f. The output voltage from the memory will be the proper amount to divert practically all of the current, furnished by the DC-offset circuit, from flowing through R_f. Subsequent samples will essentially see zero volts across the sampling gate, resulting in no change to be amplified and no change in the trace position on screen. However, the trace will be down, corresponding to a negative level at the memory output. If sensitivity is high enough to place the zero-volt level off-screen, the trace will be off-screen.

feedback path time constant

The voltage fed back and applied to the preamplifier input from the memory output, after being attenuated, has to be applied through a relatively high-resistance R_i. When the gate conducts, the voltage applied to the sampling-gate input can charge the stray capacitance at the sampling-preamplifier input rapidly compared to the rate that the voltage fed back from the memory output charges the input capacitance. The time-constant of the feedback path to the sampling preamplifier (comprised primarily of R_i and the preamplifier input capacitance) has to be chosen short enough so any output voltage step from the memory can fully charge the input capacitance to the sampling preamplifier through the resistance before the next sample is taken. But, the time-constant should not be so short that the input capacitance will lose much of its charge while the voltage across it is

being amplified, or so short that the net gain around the closed part of the loop makes the feedback regenerative. Because the maximum sampling rate is typically once every 10 μs, or longer, and the time the memory gate is conducting is typically less than 1 μs, there is at least 9 μs for the memory output to charge the sampling-preamplifier input capacitance each time a sample is taken. At least one of the amplifier stages preceding the memory gate is AC-coupled and the coupling time constant is made relatively short. In this way, each time the memory gate conducts, only the voltage from the *new* sample influences the charge stored on the memory capacitor.

Notice that the mV/DIV switch adjusts two sets of attenuators, ganged on the same switch, simultaneously. One is the forward-gain attenuator and the other is the feedback attenuator. By having these two attenuators always controlled simultaneously with the same switch, it is possible to maintain unity sampling-loop gain for all settings of the switch.

minimizing strobe signal kickout

There are several purposes for feedback. A minor one is to minimize energy being fed *out* of the vertical input connector from the push-pull strobe pulses that turn the sampling gate on and off. The sampling gate is a balanced sampling gate, one which is designed to minimize strobe-signal energy being fed back to the signal source. But how much energy is fed out is partly determined by what the signal voltage is at the time it is sampled compared to the voltage at the electrical center of the sampling gate. If both sampling-gate input diodes are back-biased at equal amounts above and below the level of the input-signal voltage when the strobe pulses arrive, the least amount of strobe signal is fed out. Remember that the center-tap voltage of the back-bias across the sampling-gate diodes may be a repeatedly changing voltage. It changes to follow every sample of the signal and is the same voltage as is attenuated and reapplied to the sampling-preamplifier input from the memory output. When loop gain is one, the voltage at the center tap is always the same as the voltage level of the input signal during the last sample. Most of the time, particularly when using the sequential mode of sample timing, successive samples represent very small differences in signal voltage level. Therefore, strobe signal kickout is minimized by continually rebalancing the sampling gate to match the last sampled signal level.

reducing vertical-deflection errors

A more important purpose of the feedback is to minimize the effects of changes in forward gain. Because the forward-gain amplifier consists of several stages, there can be a considerable change in forward gain due to component aging and temperature changes in the instrument, even though each of the stages may employ inverse feedback to stabilize the gain for that stage. The sampling loop tends to reduce errors in vertical deflection that are due to changes in forward gain. However, the tendency is not quite the same as if the feedback was the ordinary, degenerative, out-of-phase type. To understand how it does work, imagine that the forward gain has for some reason decreased by ten percent. Without feedback, the beam deflection would also decrease by ten percent and the instrument, of course, would be in error by that amount. With the feedback system, however, only a few dots in a sweep can be in error by as much as 10% if we use the sequential mode, and if sufficient dots are present in the display this error may be well under 1%. To see why this is true, imagine that we are sampling a step voltage and the first few samples have been of the baseline ahead of the step. Let's say that level is zero volts. If we also assume that the step is very abrupt compared to the time per division, and that there are no samples on the rise of the step, we have suddenly changed from sampling zero volts to sampling some positive voltage level. The first sample of the positive voltage level will cause a dot to be positioned on-screen 10% lower than it should have been. This means that the output voltage from the memory was 10% lower and the voltage fed back and reapplied to the sampling-preamplifier input was 90% of what it ideally should have been. The next sample of the same positive signal level finds the voltage at the sampling-preamplifier input 10% lower than it should have been. Had it been correct, there would have been no difference in the two levels. The remaining difference is treated as an input signal although it is actually only an error signal. The second sample of the same positive level produces a dot on the screen which goes 90% of the remaining distance, within 1% of the correct level. The first 10% error was corrected to within 1% of the correct value on the second try. By having a method of sampling which requires only that the difference between one sampled voltage and the next be processed, the difference may partly consist of errors in forward gain; and when it does, the error is minimized on subsequent samples. In the example we assumed we had

no dots on the rise. Had there been several dots on the rise of the step the dot position error would have been well under 10%. By minimizing errors in deflection in this way, we can deliberately reduce forward gain with the smoothing control, reducing random noise in the display. The smoothing control typically reduces sampling-loop gain by a factor of about 4 to 1 and this will reduce noise by about 3 to 1. The only corresponding requirement is that dot density be maintained at a high enough level to minimize dot-position errors.

offset voltage

A system which operates on the voltage difference from one sample to the next can inject an offset voltage, i.e., one which makes the input operate very much the same as a differential amplifier. The offset feature on a sampling oscilloscope is one of its main attractions because the display is almost completely free from aberrations due to overscanning the screen. Also, the offset voltage can be monitored to a fairly high degree of precision when desired.

interdot blanking

Notice now, in the block diagram, the lines coming from the blocking oscillator or avalanche driver. One line goes to the gating-pulse generator. From there a line goes to the memory gate, another to the dual-trace multi, and still another to the cathode-ray tube to produce what is called interdot blanking. The CRT beam is blanked for about one microsecond everytime a sample is taken, while the beam might be moving vertically. The purpose and effect is similar to transient blanking used in the chopped mode in conventional oscilloscopes. With this system the beam is turned on all the time except during the intervals when the dot is being changed from one position to the next and during retrace.

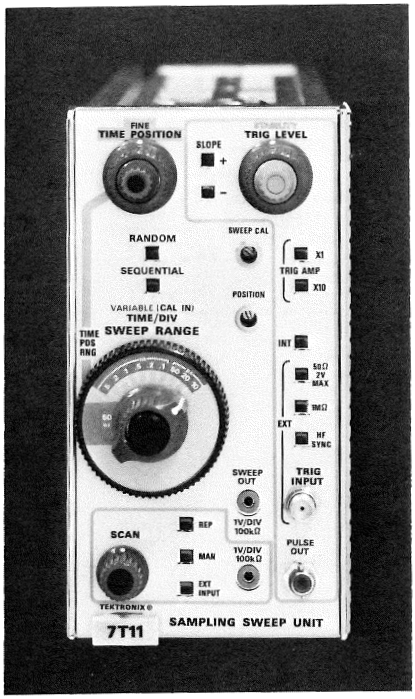
dual-trace

On sampling scopes having two input channels, instead of just a single channel as is shown in the block diagram, there are two sets of sampling-loop circuits and the output from each of the two memory amplifiers is fed to a dual-trace switching circuit ahead of the CRT vertical output amplifier. Dual-trace operation in a sampling scope is not the same as alternate-trace operation in a conventional scope. Instead the dual-trace mode is similar to the chopped mode which produces two traces in a conventional scope. Each sample of the two input signals is held in a separate memory. The output of each memory is displayed alternately on successive dots.

In the basic block diagram (Fig. 2-1), the signal which produces interdot blanking is the same one which switches the two memory outputs of a two-channel sampling scope. This dual-trace multi does not have to be synchronized with the occurrence of each sample, but when it is synchronized the job of blanking the beam while moving it is simplified.

single sweep

Whenever we produce a single sweep using a sampling scope, the number of dots displayed on-screen is equal to the number of signal cycles sampled during the sweep. In a sampling scope, single-sweep operation is not single-shot operation. We can display two traces in one sweep with an equal number of dots in each trace.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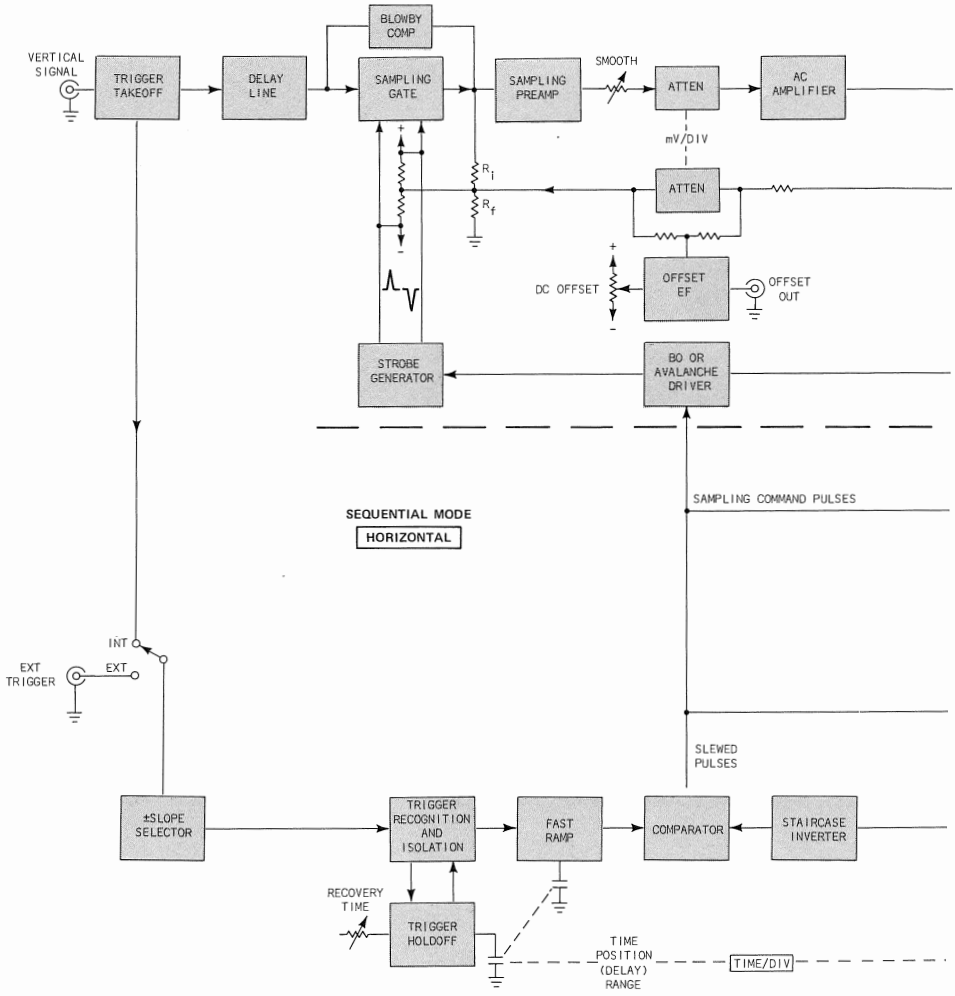
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R_i
R_f
DC OFFSET
OFFSET EF
OFFSET OUT
STROBE GENERATOR
BO OR AVALANCHE DRIVER
SAMPLING COMMAND PULSES
SEQUENTIAL MODE
HORIZONTAL
INT
EXT
EXT TRIGGER
SLEWED PULSES
±SLOPE SELECTOR
TRIGGER RECOGNITION AND ISOLATION
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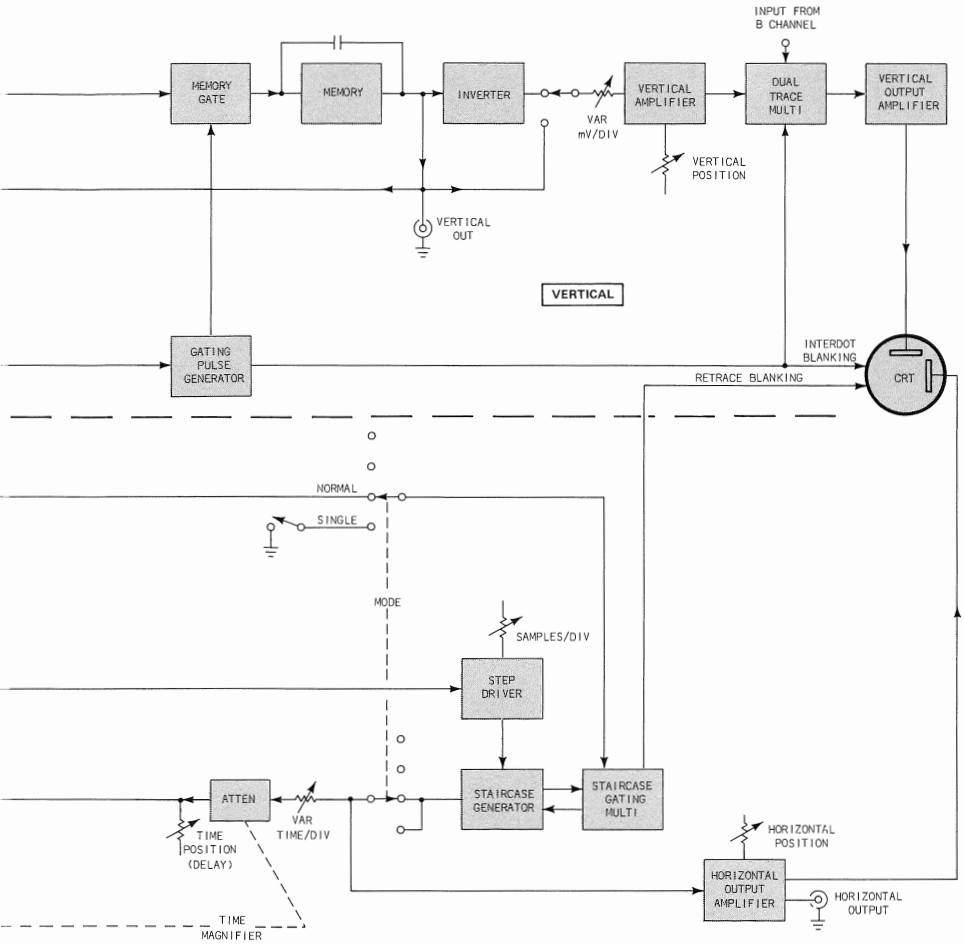
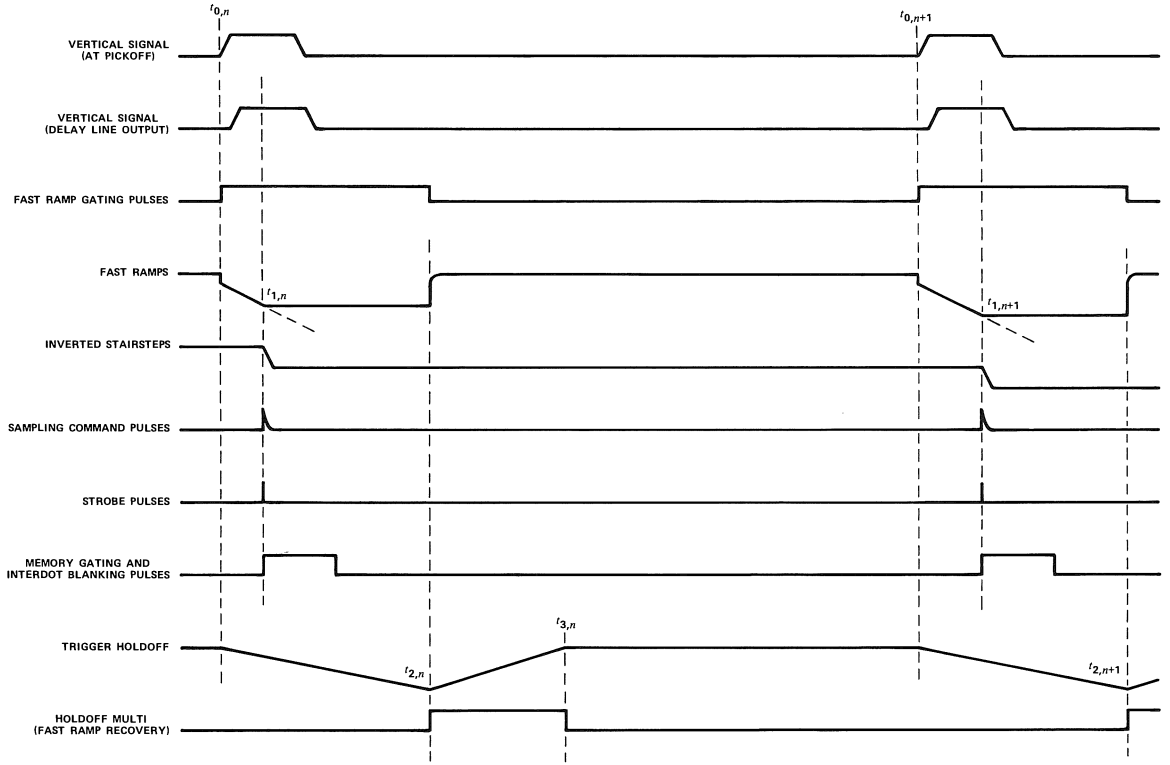


Fig. 2-3. Sequential-mode block diagram.



t_0 – THE INSTANT WHEN THE TRIGGERING SIGNAL INITIATES A FAST RAMP. EACH RAMP RUNS DOWN UNTIL IT REACHES THE LEVEL OF THE EXISTING INVERTED STAIRSTEP.

t_1 – THE INSTANT WHEN A FAST RAMP REACHES THE EXISTING INVERTED STAIRSTEP LEVEL. AT TIME t_1 A SAMPLING COMMAND PULSE, A STROBE PULSE, AND A MEMORY GATING PULSE ARE INITIATED, AND THE STAIRCASE ADVANCES ONE STEP.

t_2 – FAST RAMP STARTS TO RECOVER.

t_3 – TRIGGER HOLDOFF INTERVAL ENDS.

Fig. 2-4. Sequential-mode timing diagram.

SEQUENTIAL-MODE TIMING

This is a discussion of the function of the horizontal section of a sampling oscilloscope operating in the sequential mode, using Fig. 2-3. Fig. 2-4 shows time relationships.

triggering

Notice that, similar to conventional scopes, we must have a triggering signal in order to make a coherent display. The block diagram shows a portion of the vertical-input-signal energy diverted and delivered to the trigger-recognition block by way of the trigger slope-selection block. A suitable triggering signal from a different source might have been applied via the EXT trigger input.

fast ramp

timing ramp

slewing ramp

The function of the trigger-recognition circuit is, as the name implies, one of responding to a suitable triggering signal. The response generates a fast step-signal that initiates a ramp. This ramp can be called a fast ramp, timing ramp or slewing ramp. It is very similar in some respects to the sweep ramp in a conventional oscilloscope. One radical difference is that the slewing ramp causes no deflection. It is not applied, directly or after being amplified, to the horizontal-deflection plates. Nevertheless, this slewing ramp is one of several primary factors in a sequential-sampling time-base circuit which determine the horizontal time per division. If we steepen the slope of the fast ramp, and change nothing else, we reduce the time per division of the scale. Any nonlinearities in the slewing-ramp voltage produces a nonlinear time scale. The time-per-division on sampling scopes can be much less than on wideband conventional scopes. In wideband conventional scopes we use the fastest ramps we know how to produce, so it may be puzzling how in sampling scopes we can possibly depend on the slope of a ramp to determine the time per division. In sampling scopes, do we actually generate steeper, faster ramps than in conventional scopes? The answer is no; we don't need to. And the reason is that the ramps do not have to be very high in amplitude. In fact, to achieve less time per division on a sampling scope we only need to use *less* of a given ramp. How we accomplish this will be explained in detail later. The process is analogous to sampling a section of the timing ramps and amplifying those samples to produce horizontal deflection.

In the sequential mode, even though the horizontal position of each dot is not determined by a sample of a timing ramp, each sample does correspond to a different point on a timing ramp. In the random mode, as we will see later, the timing ramps *are* sampled, amplified and stored.

trigger holdoff

The trigger-holdoff block, just below the trigger recognition block in the diagram, represents a function which is very much the same as found in a conventional oscilloscope. That is, its purpose is to prevent the premature initiation of a new ramp excursion before the full recovery of the last one. By holding off the triggering signal or, in other words, recognizing only every cycle of the triggering signal that you can *utilize*, each fast ramp has an opportunity to fully recover and be ready to start again before a new one can possibly be triggered.

Whenever you change the time per division of the scale with a knob on the front panel, you may change one or a combination of four things. One of them is the capacitance of the fast-ramp generator. That capacitor determines the slope of a fast ramp. Another is the capacitance of the holdoff capacitor which, with the Recovery Time control, determines how far a given high-frequency triggering signal will be counted down. The third is the Display Magnifier, a gain-control switch for the horizontal amplifier. The fourth is an attenuator resistor which, as you can see, is inserted between the output of the staircase generator and the staircase inverter.

time magnification

Changing this attenuator provides what is called *time magnification*, as contrasted with *display magnification*.

The output of the staircase inverter feeds to one side of the comparator block. The other side of the comparator receives the fast ramp. Whenever a fast ramp reaches the level of an attenuated and inverted voltage, corresponding to a particular step in the staircase generator, a "slewed pulse" is produced which goes to a variety of places. The reason these

slewed pulses

pulses are called slewed pulses is that normally each successive pulse that emerges from the fast-ramp comparator is slightly later than the previous one with respect to any given point in a cycle of the signal. This slewing (or sliding) correctly implies

that each successive pulse out of the fast-ramp comparator is delayed one increment more than the former one with respect to the beginning of each fast ramp (a point in each recognized cycle of the triggering signal). A more general term for slewed pulses is sampling-command pulses.

sampling-command pulses

In a sampling scope display each dot on the screen represents a single sample of the vertical-input-signal voltage. In the sequential mode of timing samples, each successive dot on the screen is laid down from left to right in a very orderly fashion. Each new sample of the vertical signal should be a point in the signal cycle which is slightly later than the point sampled in the previous cycle. All points of interest on an input signal are sampled, in the sequential mode, by having each successive sample of each successive cycle occur slightly later in the cycle than the previous sample.

Perhaps we are now ready to see why fast ramps are also called timing ramps and sometimes slewing ramps. They have two primary functions. One function is to help determine what the time-per-division of the horizontal scale shall be. That function is the timing function. The other is to produce a series of increasingly delayed sampling-command pulses that allow us to sample all portions of the signal of interest when enough cycles have occurred. That function is the slewing function.

As you can see by the block diagram, there are two places where the slewed pulses are delivered inside the horizontal-deflection portion of the diagram. One place is to the staircase-gating multi; the other is to the step driver. The staircase-gating multi has two functions. One of them is to initiate a staircase and another is to stop the staircase after it has reached sufficient amplitude and allow it to recover.

staircase-gating multi

The staircase generator also has two functions. One of them is to produce the horizontal deflection when applied to the horizontal output amplifier. The other is to produce sets of advancing reference voltage levels, which, after being attenuated and inverted, are applied to one input of the comparator.

staircase generator

The staircase generator generates a positive staircase. That staircase is applied to the horizontal output amplifier, and produces horizontal deflection, one dot at a time. After the staircase is attenuated and inverted, it is negative-going and of less amplitude than originally. The staircase inverter is needed because the stairstep levels should advance in the same direction as the ramps, which are negative-going.

ramp versus staircase in comparator

Imagine the two inputs to the comparator: On the left-hand side is a series of negative ramp voltages; on the right-hand side is a negative staircase, a cyclic set of advancing reference levels. A new staircase level is generated each time a ramp voltage crosses the existing staircase level. Refer to Fig. 2-4. You may see that the instant when each fast-ramp crosses a new staircase level will be slightly later than the last, when compared to any given point in the sampled signal. That is because every staircase level coming into the comparator is slightly lower than the former one, and each fast ramp has to reach that level by travelling further. There is precisely one step in the staircase each time there is a fast ramp, because the slewed pulses which come out of the comparator are the *same* pulses which drive the step driver and cause the staircase generator to advance one step. Every time the staircase generator advances one step, an inverted step of proportional size is applied to the right-hand side of the comparator and becomes the new reference level which the subsequent fast ramp must cross to produce the next slewed pulse.

staircase reset

After enough steps have been generated so that the staircase amplitude reaches a predetermined voltage, the voltage necessary to produce full-scale horizontal deflection, the staircase-gating multivibrator turns off the generator, allows it to recover and be readied for a new staircase. Any fast ramps which are generated during the time when the staircase generator is recovering will also cause slewed pulses to be produced and samples of the signal taken, but these samples will not be shown on-screen because the staircase-gating multivibrator blanks the CRT during the retrace period. The retrace period is the time when the staircase generator is recovering and getting ready to generate another staircase.

dots per division

Let's consider that we have a 50-volt staircase which has a thousand steps, resulting in a thousand dots across the ten-division screen. This is 100 dots per division. Let us also assume that the ramp voltage goes from zero to ten volts negative. If we were to attenuate the staircase generator by a factor of ten the output of the staircase inverter would be a smaller staircase that went from zero to five volts negative. The 0 to -5 volt excursion of the inverted staircase would be only one-half of the 0 to -10 volt amplitude of the ramp. Also, in that 0 to 5 volts there would be 1000 separate discrete levels applied to the comparator during the time when the staircase generator was running up. That is to say, each discrete level of the inverted staircase would only differ from the next by one-thousandth of five volts, or five millivolts. Now if the slope of the 10-volt ramp were such that it took 100 nanoseconds to go from 0 volts to 10 volts, we may see that any 5-volt segment of the 10-volt ramp will occur during 50 ns. If we assume that the first dot laid down on the screen corresponds to a time when a fast ramp crossed a minus 1-volt level coming from the staircase inverter and the last dot on screen corresponds to the time when a fast ramp crossed a minus 6-volt level coming from the staircase inverter, you may see that in terms of one fast ramp only, the time between the first dot on screen and the last on screen corresponds to 50 ns. Now it is true that 1000 fast ramps had to occur before we would get 1000 dots on the screen, but in terms of just the increments of delay of each successive slewed pulse from first to last, we would have 1000 increments totaling 50 ns.

time per division

This would tell us that the time per division of a ten-division horizontal scale would be 5 ns.

If we remember that there are 100 dots for every division, then we can figure that the time represented by the distance between each successive dot is 1/100th of 5 ns, or 50 ps. Now the time represented by the distance between dots at this point is not very significant, but it is interesting to note that the 50 ps represented by the distance between dots corresponds to the real time it takes for a fast ramp to change 5 mV. In other words, the time it takes a ramp of that slope to move 5 mV is 50 ps. The 5 mV figure, remember, was the difference in staircase level from one step to the next at the input to the comparator. If the sweep were comprised

of less than 1000 dots, then the time represented by the distance between dots would be greater than 50 ps, but the time represented by one centimeter on the scale would remain unchanged at 5 ns.

As mentioned earlier, one of the things which determines the time per division of the horizontal scale is the amount of attenuation between the staircase generator and the staircase inverter. If we were to attenuate the staircase by a factor of 100, instead of by a factor of 10 such as we chose in the example in the last paragraph, then the difference in level between each successive step out of the staircase inverter would be only 1/10th of 5 mV, or 500 μV. Then the time it takes one fast ramp to go between one level and the next would be 1/10th of what it was formerly. The full 10-division scale, instead of corresponding to 5 volts of the fast ramp, would now correspond to only 1/10th of that or 0.5 volts. In this case the time-scale would be 0.5 ns/div instead of 5 ns/div and the 10-division scale would be 5 ns. Simply by attenuating the staircase fed into the comparator, we can make a given ramp produce a time-scale that represents less time per division. However, carefully notice that the staircase which goes to the horizontal amplifier is *not* attenuated. It always remains adequate to produce full-scale deflection. Had it been attenuated by the same factor (10X) there would have been only one division of deflection instead of ten and *no* change in the time represented by that division.

time/div independent of dots/div

It is important to mention again that in the sequential mode, whether we have a 1000-dot sweep or a sweep with some other number of dots, the time per division of the scale does not change. (However, the time it takes the beam to move one division *will* change.) The reason the time scale doesn't change is that when the staircase steps are large and produce a correspondingly large horizontal separation between dots, they also produce a proportional change at the comparator input. For example, if instead of having a 1000-step staircase, we changed the samples per division at the step driver so that we had a 500-step staircase, then each level fed to the comparator after being inverted by the staircase inverter would not be 5 mV, as we chose originally, but 10 mV. The

time represented by the distance between dots then would be 100 ps instead of 50 ps, but because there are only 50 dots per division now, instead of 100 dots per division, we still would have 5 ns per division.

time position

Notice the time position control inserted between the staircase inverter and the attenuator leading into it. The time position control on a sampling scope is the same sort of thing as a sweep delay control in a conventional scope, except that the rotation of the dial clockwise produces a movement of the display to the right, the opposite direction from what we're used to for a delay control, but the direction you might expect. Time position seems to be an obvious term if you imagine the CRT screen as a sort of port or window through which a portion of the graphic history of a changing voltage may be viewed. What the time position control does in the circuits is to apply an offsetting DC current at the input of the staircase inverter, so that the output level of the entire inverted staircase may be varied. Typically, the time position control allows us to move the level of the inverted staircase by up to half of the voltage of a full excursion of the fast ramp. In the example we said the fast ramp had a 10-volt excursion, and we said the attenuated and inverted staircase had a 5-volt excursion. If, using the time position control, we can make the first staircase step at the output of the staircase inverter be anywhere from 0 to -5 volts, the last step would end somewhere between 5 and 10 volts. By this means we utilize the fast ramp to produce delay, as well as perform its other functions. Whenever we have the time position control rotated fully clockwise, we have minimum delay and the display on the screen moves to the right as far as possible. In the other extreme, if the time position control was rotated fully counterclockwise, delay would be a maximum and the display on screen would move as far to the left as possible. Under the latter conditions, the staircase would start at -5 volts and move down to -10 volts. You may see then that each fast ramp must move at least 5 volts in order to reach a voltage level fed into the comparator from the staircase inverter. The first dot on-screen would then correspond to a delay equal to 5 volts on the fast ramp, or 50 ns of delay.

This completes a description of the fundamental concepts of the conventional sequential mode of sampling. The method of relating all the horizontal positions of the beam to corresponding points on a fast ramp is unique to this mode. And the technique of delaying the strobe pulses by discrete time-increments which are related jointly to the slope of the fast ramp and the position of the beam is also unique to this mode. The 7T11 Time Base unit has some variations, however.

7T11 SEQUENTIAL-MODE PRINCIPLES

Refer to the simplified block diagram on the opposite page.

Each time the input triggering signal is recognized, both a slewing ramp and a timing ramp are initiated simultaneously. Each slewing ramp runs down until, as it crosses the ramp level that exists at the output of the slow ramp generator, it generates a sampling-command pulse. Each sampling-command pulse stops the run-down of the timing ramp and causes the vertical input signal to be sampled. The stopped level of each timing ramp is transferred to a horizontal memory and causes horizontal deflection proportional to the stopped level.

Unlike the more conventional method of sequential sampling, the horizontal position of each dot is not *pre*determined by a staircase generator. If a sampling-command pulse is generated a little earlier or later than it ideally should occur, because of inherent noise in the comparator, the timing ramp will be stopped early or late by the same amount, reducing time jitter in the displayed signal. The horizontal spacing between successive dots may change, therefore, and corresponding dots in successive sweeps may not precisely overlap.

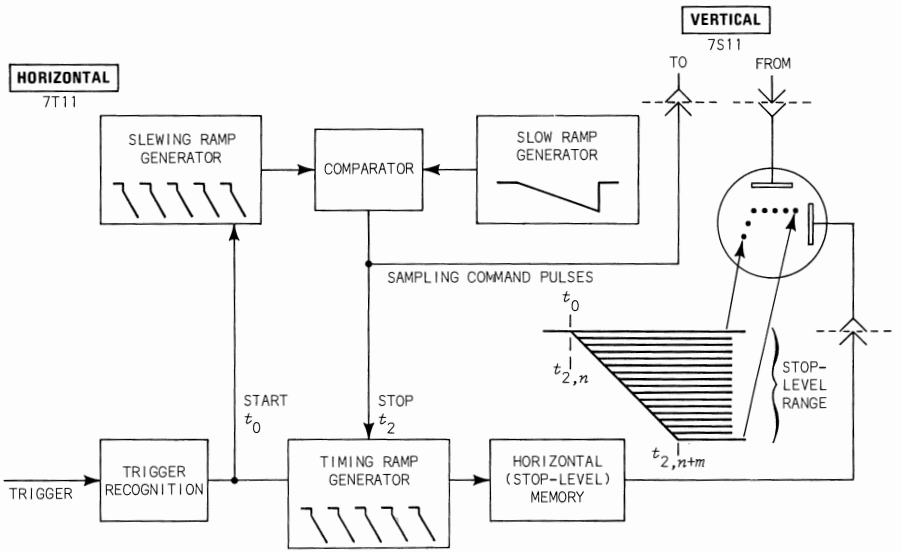
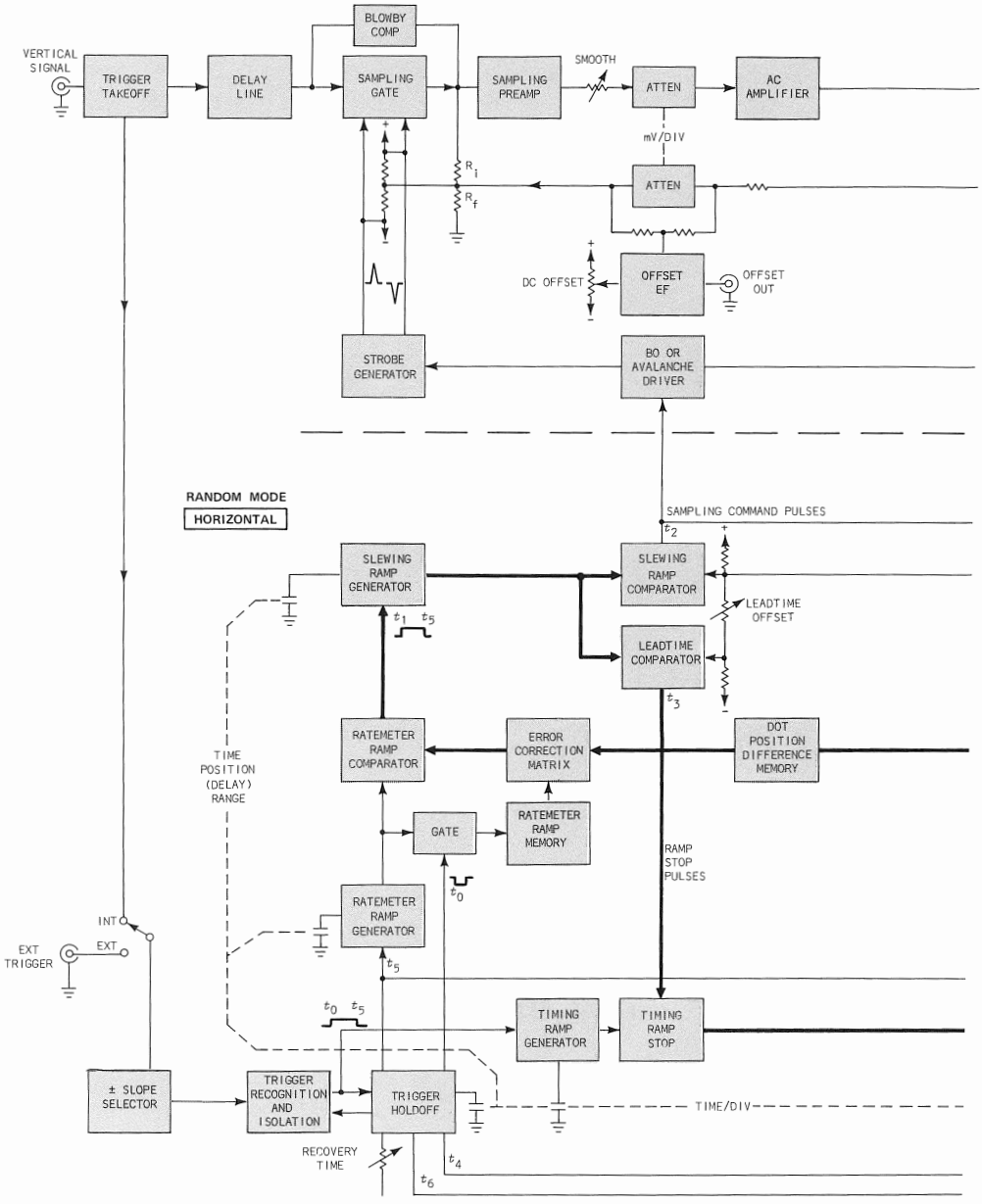


Fig. 2-5. 7T11 sequential mode (simplified).


VERTICAL SIGNAL
TRIGGER TAKEOFF
DELAY LINE
BLOWBY COMP
SAMPLING GATE
SAMPLING PREAMP
SMOOTH
ATTEN
AC AMPLIFIER
mV/DIV
ATTEN
R_i
R_f
DC OFFSET
OFFSET EF
OFFSET OUT
STROBE GENERATOR
BO OR AVALANCHE DRIVER
RANDOM MODE
HORIZONTAL
SAMPLING COMMAND PULSES
t_2
SLEWING RAMP GENERATOR
SLEWING RAMP COMPARATOR
LEADTIME OFFSET
t_1 t_5
LEADTIME COMPARATOR
t_3
RATEMETER RAMP COMPARATOR
ERROR CORRECTION MATRIX
DOT POSITION DIFFERENCE MEMORY
TIME POSITION (DELAY) RANGE
GATE
RATEMETER RAMP MEMORY
RAMP STOP PULSES
t_0
RATEMETER RAMP GENERATOR
INT
EXT
EXT TRIGGER
t_5
t_0 t_5
TIMING RAMP GENERATOR
TIMING RAMP STOP
± SLOPE SELECTOR
TRIGGER RECOGNITION AND ISOLATION
TRIGGER HOLDOFF
TIME/DIV
RECOVERY TIME
t_4
t_6

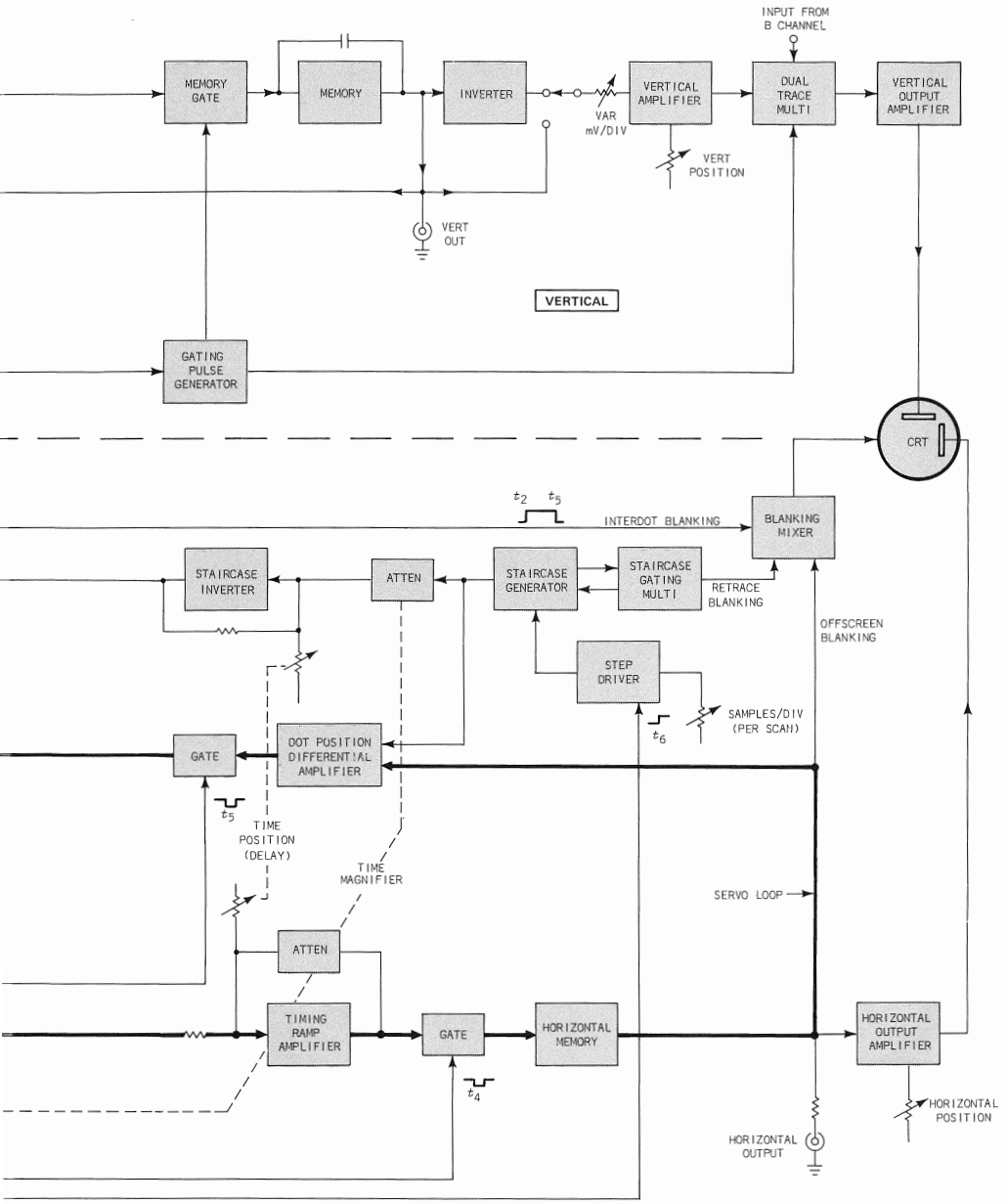


Fig. 2-6. Random-mode block diagram.

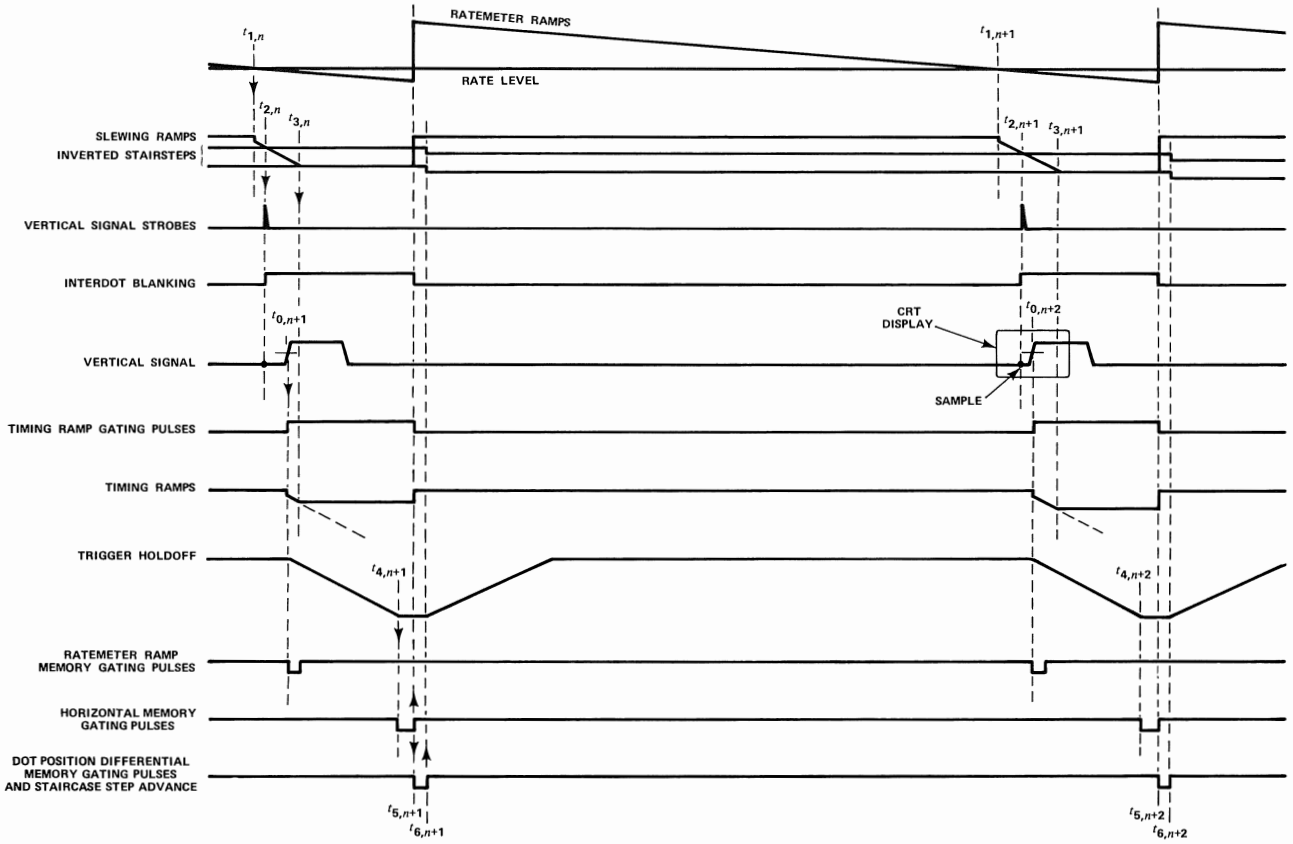


Fig. 2-7. Random-mode timing diagram.

RANDOM-MODE TIMING

Random sampling is one of the basic modes of strobe timing used in sampling oscilloscopes. A good understanding of the sequential mode discussed earlier in this chapter is required for this discussion. The two strobe timing methods for the real-time mode are discussed in the last part of this chapter.

random dot sequence

The random mode is not simply a mode for sampling a signal which occurs at a random rate and producing a coherent graphic display from such samples. The sequential mode actually handles signals of that character better than the random mode. The use of the word random pertains to what appears to be an absence of order in the sequence in which dots occur on the screen, and to the fact that the sampling command pulses do not have to be precisely synchronized with the signal being sampled. The timing ramps *are* still triggered in precise synchronism with the signal cycles, however.

When the sampling command pulses are not precisely synchronized with the signal cycles, each sample will produce a dot which may occur on the screen either to the left or to the right of the previous sample, without effecting the coherence of the display. The dots laid down on the screen, therefore, appear to be at random compared to the sequential mode. The degree of randomness is a function of signal-cycle jitter and jitter of other kinds. No deliberate attempt is made to sample in a random fashion. Because the dots are not laid down from left to right across the screen in a completely orderly sequence does not mean that each dot cannot be in its correct position. Plotting any graph, point by point, can be done just as well by jumping around at random as when done in a more orderly manner as long as each dot is plotted at the *correct* X and Y coordinate position.

eliminates delay line or pretrigger need

The *advantage* of the random mode of sampling does not pertain to randomness of any kind in any way. The advantage of random sampling is that it is a way of sampling and viewing sections of a signal ahead of the trigger-recognition point (usually on the leading edge of a pulse) without the use of vertical signal delay lines or an externally-applied pretrigger signal. pretrigger signal.

When we use sweep delay in a conventional oscilloscope to view portions of a signal ahead of the trigger-recognition point, we sometimes may accomplish the same sort of thing. When we do, we depend first of all on the fact that the signal is recurrent. Whenever a signal is recurrent we can trigger a delay generator with one occurrence of a signal cycle, and with the delay generator cause a subsequent trigger pulse to be generated *ahead* of the next occurrence of the signal cycle, the one to be viewed. When we do this, we are essentially generating our own pretrigger signals and this is basically the same process we use in the random sampling mode. But there are two big differences in the analogy. First of all, in a sampling oscilloscope operated in the random mode, we use a system of automatically metering the signal cycle repetition rate so as to produce delayed triggers which occur at the same rate or a submultiple of the same rate. But the main difference is that time-jitter, due to either scope delay-jitter or signal-cycle jitter, *does not show up as a blurred display*. Instead, such jitter merely affects the degree to which successive dots appear to occur in random positions. We trade what would be a jittery, blurred, incoherent display for one which is coherent by allowing the jitter to manifest itself in the randomness of dot positions. This process is not the same as using a delayed trigger merely to arm the trigger recognition circuits. That process still relies on the use of a vertical signal delay line to view sections ahead of the trigger recognition point.

delayed triggers

jitter

The underlying principle of trading delay jitter for randomness of the point-by-point plot is that both the vertical signal *and* a triggered linear timing ramp corresponding to a sweep are sampled each time a dot is displayed on the screen. Because each timing ramp is triggered by the same point in each cycle of the signal which is sampled, the proper X and Y coordinates for each dot are available at the output of the vertical memory and the horizontal memory. In the sequential mode no ramp is sampled, only the vertical signal is sampled.

timing ramp is sampled

Refer to the double-page block diagram, Fig. 2-6. Notice that in the random mode *two* kinds of sampling-command pulses are generated. One goes to the vertical-deflection section of the scope to cause the vertical signal to be sampled, and one stays in the horizontal-deflection section to cause the timing ramps to be sampled. The ramp-stop pulses cause the timing ramps to be sampled. In the random mode, two separate and distinct sampling processes go on continually; one for the vertical signal and one for the timing ramps. The sampling-command pulses for the timing ramps are called ramp-stop pulses. Samples of the timing ramps are amplified and stored in the horizontal memory. From there they are amplified and produce horizontal deflection in very much the same way as the output from the vertical memory produces vertical deflection.

In the sequential mode of operation, you may recall, the fast ramps perform two functions. One, the timing function, is to help determine the time per division of the horizontal scale and the other, the slewing function, is to produce various increments of strobe delay so that all portions of the signal to be sampled will be sampled and displayed. In the random sampling mode these two functions still must be performed. One is performed by fast ramps from one fast-ramp generator and the other is performed by fast ramps from a second fast-ramp generator. Both ramps have precisely the same slope and have the same repetition rate but start at different moments. One of these fast ramps is called the timing ramp and the other is called the slewing ramp.

two fast-ramp generators

Now the main purpose of the random sampling mode, remember, is to reduce the need for a vertical signal delay line when no pretrigger signal is available. To do this it is necessary to generate our own pretriggers. However, unlike the usual pretrigger, the ones that we *generate* in the random mode do not have to occur precisely the same amount of time ahead of the section of the signal to be displayed each time they occur. That is because there are *two* related but separate triggered functions in sampling scopes but only *one* in a conventional scope. In a

pretriggers

conventional scope we only need to trigger a sweep ramp. In a sampling scope we must not only trigger a timing ramp but we must also trigger the strobe pulses that sample the signal to be displayed. In the random mode we trigger the timing ramps in the usual way and with the internally generated presignal triggers cause the strobe pulses to be generated. But the strobe pulses are not triggered directly by the presignal triggers but are triggered after being increasingly delayed (slewed) with reference to the presignal triggers.

In both the sequential mode and the random mode the instant when the timing ramp triggering signal is recognized defines the trigger-recognition point (t_0) on the vertical signal. Whether the timing ramp triggering signal is a portion of the vertical input signal or an externally applied triggering signal is immaterial. In the random mode an externally applied triggering signal may be used that lags the leading edge of the signal to be displayed. In that case the trigger recognition point would be later than the leading edge but points ahead of the leading edge could still be sampled and displayed.

Let's look at the block diagram (Fig. 2-6) and note some similarities between the random mode of operation and the sequential mode. First of all notice that, as with the sequential mode of operation, only two signal lines go between the vertical and the horizontal sections of the block diagram. The one at the far left is the signal line which carries the trigger-pickoff signal from the vertical-signal input to the trigger-recognition block at the bottom left-hand corner of the diagram. Going from the horizontal section to the vertical section are the sampling command pulses from the slewing-ramp comparator. In the bottom left-hand corner of the diagram we see the trigger-recognition block and the trigger-holdoff block, both of which are common to the sequential mode of operation. The primary signal out of the trigger-recognition block is the step signal which initiates the timing ramp in the timing-ramp generator. This also is common with the sequential mode of operation, except the timing ramp is called either a fast ramp or a slewing ramp. As mentioned earlier, the slewing function is performed by a slewing ramp. It has the same slope as the

timing ramp. The slewing-ramp generator block is in the upper left-hand side of the horizontal section of the block diagram. The slewing ramp drives the slewing-ramp comparator in the same way that the fast ramp drives the fast-ramp comparator in the sequential mode diagram. The voltage levels against which the slewing ramps are compared are negative levels which arrive from the output of the staircase inverter. The staircase inverter is driven by a positive-going staircase, which is first attenuated before being applied to the staircase inverter.

One big difference in the random mode of operation is that the staircase generator does not produce any horizontal deflection. The sole purpose of the staircase generator is to help the slewing ramps produce sampling-command pulses and ramp-stop pulses that sample all portions of the vertical signal and timing ramps.

The staircase-gating multi and the step-driver have functions similar to that of the sequential mode.

Six of the blocks in the horizontal section of this block diagram have functions which are involved with nothing except generating presignal triggers. The names of the six blocks are: Ratemeter ramp generator, ratemeter ramp memory, ratemeter ramp comparator, error correction matrix, dot position difference memory and dot position differential amplifier. A discussion of the functions represented by those blocks will be postponed while we give our first attention to the other blocks.

We said that the slewing ramps, in the upper left-hand corner, drive the slewing-ramp comparator to produce sampling-command pulses for the vertical section. Notice, also, that the slewing-ramp generator drives another kind of comparator called the leadtime comparator. The stepped reference voltage levels for both of these comparators are the inverted staircase levels that correspond to the staircase steps after being attenuated. The output of the staircase inverter is a negative-going staircase. Notice that the negative-going staircase, before being applied to the leadtime comparator, is offset further negative by the voltage drop across the resistor labeled leadtime offset. In an actual circuit a constant current flows through that resistor producing a constant voltage drop.

leadtime comparator

The slewing ramps, the same as the fast ramps in the sequential mode, are negative-going ramps. But unlike the sequential mode, two pulses are produced every time a slewing ramp occurs instead of just one pulse. The first emerges from the slewing-ramp comparator. The second emerges from the leadtime comparator. The sampling-command pulses which come from the slewing-ramp comparator always cause the vertical input signal to be sampled and that is always sooner than the ramp-stop pulse samples the timing ramps. A pulse edge from the leadtime comparator stops the timing ramp at whatever voltage the ramp had reached at the moment the pulse edge occurs, and that level remains constant until the timing-ramp gating pulse ends and the ramp starts to recover. This manner of stopping the timing ramp and causing it to remain at the level at which it stopped is the process of sampling the timing-ramp signal. The stopped amplitude of each timing ramp is a good *sample* of the amplitude that existed at the moment the stop-pulse arrived from the leadtime comparator. Do not misunderstand the function of the leadtime comparator. Leadtime is the amount of time ahead of the trigger-recognition point that we may sample and display the vertical signal. The pulses which emerge from the leadtime comparator *always follow* the pulses which emerge from the slewing-ramp comparator. However, the difference between the instant when each sampling-command pulse is generated and the subsequent instant when each timing-ramp-stop pulse is generated determines the leadtime. Adjustment of the Leadtime Offset control, an internal adjustment, determines the difference in the reference voltage levels that are applied to the two comparators from the staircase inverter. The difference in level determines the difference in time between the generation of a sampling-command pulse and the generation of a ramp-stop pulse, and this determines the leadtime.

sampling-command pulse

timing-ramp-stop pulse

leadtime determination

Each stopped timing ramp is amplified and inverted by the timing-ramp amplifier and applied to a horizontal memory. The output of the horizontal memory, after being amplified by the horizontal-output amplifier, determines the horizontal position of any dot on the screen. Under ideal circumstances the dots which are laid down on the screen simulate the

horizontal dot position

appearance of the sequential mode, where they are laid down from left to right in equal steps from the output of the staircase generator. But the horizontal position of any dot is not *controlled* by the staircase generator. Instead it is controlled by the voltage at the output of the horizontal memory.

time-per-division controls

The time per division for the horizontal scale for the random mode is controlled from the front panel by three controls. One of them determines the slope of the timing ramp, one determines how much amplification we use ahead of the horizontal memory and one controls the gain of the horizontal amplifier. The TIME MAGNIFIER controls the amount of amplification, TIME POSITION RANGE control determines the slope of the timing ramp, and a control called DISPLAY MAG determines the gain of the horizontal amplifier.

The horizontal deflection system for the random mode of operation is very similar in many respects to the conventional oscilloscope sweep generator and sweep magnifier. It is not at all like the sequential-mode deflection system. In a conventional scope the fastest sweep is generally achieved by the process of amplifying a small portion of the fastest sweep ramp. Almost exactly the same sort of thing occurs in the random sampling mode, except that by sampling the timing ramp before amplifying it we may amplify it with amplifiers having a low bandwidth and thereby easily achieve less time per division for the horizontal scale. In the 3T2, for example, the time magnifier can magnify the fastest timing ramp 50 times, and the fastest timing ramp *without* magnification is 10 ns per division. How short the time per division might be is limited only by what practical use might be made of extremely short time-scales and how much display time-jitter you are willing to tolerate. Light travels one centimeter in 33 ps in air and it is common for the shortest time per division to be equivalent to a 20 ps per centimeter rate or faster.

short time-scales

As long as the vertical signal and the timing ramps are locked together, simultaneously sampling those two signals should result in two samples that bear the correct *X* and *Y* coordinate relationship to each other, regardless of when the samples are taken.

This is when the samples are taken simultaneously. What if they are not taken simultaneously but one sample is taken before the other? Even then it doesn't matter so long as the time between each pair of samples remains unchanging. See Fig. 2-7. When a sample of the vertical signal precedes a sample of the timing-ramp signal by the same amount every time the two signals are sampled, the display will be just as correct and coherent as if the pairs of samples always occurred simultaneously. The difference will be that *a sample of the signal taken prior to the trigger-recognition point on the vertical signal may be displayed.* Samples taken after the trigger-recognition point may also be part of the display. This difference is in our favor and what makes random sampling useful. How much time the vertical signal may be sampled ahead of the trigger-recognition point and still be correctly displayed, will be the time between the instant when the vertical signal is sampled and the instant when the timing-ramp signal is sampled. This selectable but fixed interval of time is leadtime. In the 3T2 the leadtime is equal to six-tenths of the selected time position range and amounts to at least six divisions of the ten-division scale except for the 100 ns range.

leadtime

Let us now consider in detail the functions of the six blocks which are involved with the generation of pretriggers. First of all, notice the lines in Fig. 2-6, identified by t_0, t_1, t_2, t_3, t_4, t_5 and t_6. These lines all deliver pulses. The pulse *edges* that we are concerned with occur at instants in time identified as t_0, t_1, etc. In every normal sampling cycle the order of the occurrence of the instants t_1 through t_6 is the same. However, the trigger-recognition point t_0 may occur either before or after time t_1 in any normal cycle. Even though this is so, all pulses actually depend on the generation of trigger-recognition pulses at time t_0. That is because a pulse edge at time t_0 in one cycle initiates events which always cause a delayed pulse to be generated at time t_1 in the *next* cycle. See Fig. 2-7.

Time t_0 is the trigger-recognition point, the master time-reference point in each sampling cycle. The sequence of events initiated at t_0 set the stage for each subsequent sampling cycle. The pulse edge at time t_0 causes a timing ramp to be initiated, and causes the existing ratemeter-ramp level to be gated into the ratemeter-ramp memory.

Time t_1 occurs when the ratemeter ramp crosses a level introduced to the ratemeter-ramp comparator from the error-correction matrix. The pulse edge at time t_1 causes a slewing ramp to be initiated. Ideally, time t_1 is a stable pretrigger point which occurs well ahead of time t_0 in *that* sampling cycle. In the first sampling cycle no event occurs at t_1, t_2 or t_3.

Time t_2 occurs when a slewing ramp crosses the level introduced to the slewing-ramp comparator from the staircase inverter. The pulse edge at time t_2 is a vertical-signal sampling command and, essentially, is the instant the vertical signal is strobed and sampled.

Time t_3 occurs when a slewing ramp crosses the lower negative offset level which rides on the output from the staircase inverter. It occurs at a fixed time interval following t_2. The pulse edge at time t_3 is a timing-ramp sampling command that stops the timing ramp in its run down and holds that level as a sample until amplified and stored in the horizontal memory.

Time t_4 occurs at the end of the first part of the holdoff cycle. The pulse beginning at time t_4 and ending at time t_5 gates the amplified, stopped level of the timing ramp into the horizontal memory.

Time t_5 occurs shortly after time t_4 at the middle of the holdoff cycle. The pulse edge at time t_5 resets the timing-ramp generator, the slewing-ramp generator and the ratemeter-ramp generator (which starts over again automatically). The pulse beginning at time t_5 and ending at time t_6 gates into the dot-position difference memory whatever voltage may be applied at that moment from the dot-position differential amplifier.

Time t_6 occurs a moment later than t_5 during the last part of the holdoff cycle. The pulse edge at time t_6 causes the staircase generator to advance one step.

ratemeter ramp

Let's look at the ratemeter-ramp generator block (Fig. 2-6). The ratemeter ramp is a relatively slow ramp. It has an excursion which may last 1000 times as long as the time position range and is selected with the same control. Whenever a ratemeter ramp is initiated, as with the generation of a pulse edge at time t_5 from the trigger-holdoff block, the ramp starts a slow rundown. It runs down until the next similar pulse edge at time t_5 emerges from the trigger-holdoff block. At that moment the ratemeter ramp reverts and starts over again at the same slope. The ratemeter-ramp amplitude, therefore, is a function of the time between occurrences of successive pulse edges at time t_5. In other words, the ramp amplitude is a function of the trigger-recognition rate. Remember, this rate may not be the same as that of the triggering signal if the triggering signal is a high-frequency signal and trigger countdown is occurring.

The ratemeter ramp goes two places, to the ratemeter-ramp comparator and to the ratemeter-ramp memory. The ratemeter-ramp amplitude at time t_0 is stored in the ratemeter-ramp memory. At time t_5 in every cycle the ratemeter ramp resets and starts down again. The ramp amplitude stored in memory will be an unchanging DC level if the trigger-recognition rate is a very constant frequency. If the frequency decreases, the ramp amplitude increases and the rate level increases in the negative direction. The level out of the ratemeter-ramp memory is mixed with another level in the error-correction matrix and the combination is fed over as a reference level for the ratemeter-ramp comparator.

Let's consider for a moment that the level fed out of the error-correction matrix to the ratemeter-ramp comparator is slightly higher by a fixed amount than the level out of the ratemeter-ramp memory. Such a condition is normal and typical because of the other servo-loop input to the error-correction matrix.

When a down-going ratemeter ramp, which is fed into the ratemeter-ramp comparator, reaches this level the leading edge of an output pulse will emerge which initiates a slewing ramp in the slewing-ramp generator. Because the reference level at the input to the ratemeter-ramp comparator was slightly higher than the level out of the ratemeter-ramp memory, the negative-going ratemeter ramp will cross this level *sooner* than if it ran all the way down to the level that is *at* the output of the ratemeter-ramp memory. Because the level at the output of the ratemeter-ramp memory is the level of the ratemeter ramp when last sampled at time t_0, the pulse which emerges from the ratemeter-ramp comparator will normally occur ahead of each new time t_0. That pulse is our pretrigger pulse. The pretrigger pulses occur at time t_1 and start the slewing ramps. Remember the pulses generated at time t_1 occur as a result of events in the *previous* cycle, and in that way can occur prior to time t_0 in any given cycle.

pretrigger pulse

As a slewing ramp runs down it first produces an output pulse at the slewing-ramp comparator, then produces an output pulse at the leadtime comparator. The first pulse causes the vertical signal to be sampled, the second pulse causes the timing ramp to be sampled. With these two samples we have enough information to correctly position one dot on-screen, both vertically and horizontally.

Now if the slewing-ramp comparator and the leadtime comparator did not have changing reference levels fed into them from the staircase inverter, each of the pairs of pulses produced by each slewing ramp crossing the two levels might sample the signal and a timing ramp at nearly the same point each cycle. This condition isn't desirable because we need to sample the vertical signal at all points of interest in order to display all points of interest. So we must have a slewing function. This slewing function follows the same pattern as occurs in the sequential mode of operation. That is, we generate a series of staircase levels which are applied to the slewing-ramp comparator and these changing reference levels, which step once with every sample, cause us to slew

slewing

across the entire signal and sample all portions of it after enough slewing ramps have occurred. We *try*, therefore, to sample the vertical signal in exactly the same manner as though we were sampling it in the sequential mode, except we start to slew from a point *ahead* of the trigger-recognition point.

To help simulate that process, the level out of the staircase generator at any moment, which corresponds in one sense to a particular spot on the horizontal scale, is applied as one input to the dot-position differential amplifier. The other input to the dot-position differential amplifier is the output of the horizontal memory. If a particular sample was placed on the screen at the same horizontal position as the staircase generator would have placed it had we been sampling in the sequential mode, there would be no difference in the voltage from the staircase generator compared to the output voltage from the horizontal memory. If there is no difference in dot position, then there will be no error signal to store in the dot-position difference memory and no error signal level added to or subtracted from the level corresponding to the stored ratemeter-ramp amplitude applied to one input of the error-correction matrix.

error signal

Typically, the horizontal position of any one dot may differ radically from the position that dot would have if it had been placed there by the staircase generator. If the position of a dot is further to the right on the screen than it ideally should be, then there will be one polarity of voltage applied to the dot-position difference memory. If the dot is further to the left than it ideally should be, then there will be the opposite voltage applied to the dot-position-difference memory. The polarity and the magnitude of the voltage which comes out of the dot-position-difference memory has a direct influence on the DC level which comes out of the error-correction matrix and is applied as a reference level at one input to the ratemeter-ramp comparator. A change in the DC level of this reference input will cause the pretrigger signal to occur earlier or later than it formerly did to minimize the error and repeatedly sample the signal most of the time over the particular region to be displayed on screen. The process is one of

horizontal dot-position determination

continually metering and correcting for errors in the estimation of the trigger-recognition rate so as to produce pretriggers at the same rate, and at times (t_1), which are consistently early by a nearly constant amount compared to the trigger-recognition point (t_0).

blanking

CRT beam blanking and unblanking is different from the sequential mode. In the sequential mode the beam is blanked for the same time interval each time a new sample is taken. Those moments are when the memory is charging and the staircase generator is stepping. In the random mode a sample of the vertical signal is always taken before a sample of the ramp signal is taken. So the beam must be blanked at least between the moment when a new sample is placed in the vertical memory and a corresponding sample is placed in the horizontal memory, or each vertical sample will appear at two horizontal positions. Actually the beam is blanked a little longer than that and the time varies. Blanking occurs between the moment when the vertical signal is sampled (t_2) and the last moment when the timing ramp may be sampled (t_5). The beam is also blanked during the time the staircase generator is recovering and any time when output from the horizontal memory would otherwise place a sample off-screen.

To summarize: Random sampling is a mode where we not only sample points of interest in successive cycles of a repetitive vertical input signal but also synchronously sample corresponding points on a triggered linear ramp. The samples of the vertical signal produce vertical deflection proportional to the voltage of the signal at the instants when sampled and the samples of the ramp signal produce horizontal deflection proportional to the voltage of the ramp signal at the instants when sampled. This process permits each sample of the vertical signal to be *independently* plotted at the correct horizontal position regardless of the horizontal position of the previous sample. That permits an imperfect prediction system to generate presignal triggers that are practically perfect, as long as most of them cause strobe pulses to occur close enough to the signal to be within the time interval represented across the screen. In order

to *display* portions of a signal ahead of the trigger recognition point, the strobe pulses that sample the vertical signal must occur a fixed interval of time ahead of those that sample the linear ramp. The ratemetering (prediction) system, first of all, uses a time-to-height converter to produce a voltage level proportional to the intervals of time between (recognized) cycles of the vertical signal. This voltage level is stored in the ratemeter memory capacitor. An additional corrective servo-loop modifies that level so that strobe pulses occur not only at the trigger recognition rate but at the right instants to sample the vertical signal at the points of interest.

The 7T11 Time Base unit employs some random mode principles that differ from those discussed so far.

7T11 RANDOM-MODE PRINCIPLES

Refer to the simplified block diagram on the facing page.

After the input triggering signal is applied and its cycles are repeatedly recognized and metered several times, the instants of trigger recognition may be predicted. Pulses that occur at the recognition rate are then produced by the internal pretrigger generator and are made to occur just prior to the instants when each cycle of the triggering signal occurs and is recognized. It is not necessary for each pretrigger to occur early by precisely the same amount of time each time one is generated. Each pretrigger pulse initiates a slewing ramp and enables a timing ramp to be generated. At the instant when each slewing ramp crosses the level that exists at the output of the slow ramp generator, a sampling-command pulse is generated.

After the timing ramp generator is enabled, a timing ramp is initiated at the instant when a sampling-command pulse is generated or at the instant of trigger-recognition -- whichever occurs first. At the second instant, the timing ramp is stopped. Ramp amplitude, therefore, will be proportional to the interval of time between when the vertical input signal is sampled (t_2) and when the triggering signal is recognized (t_0).

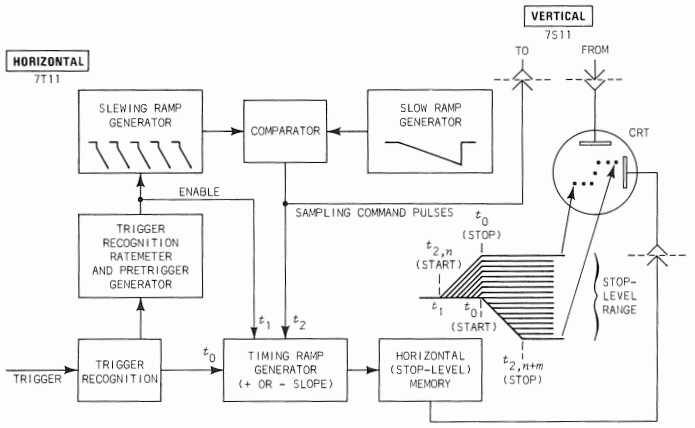
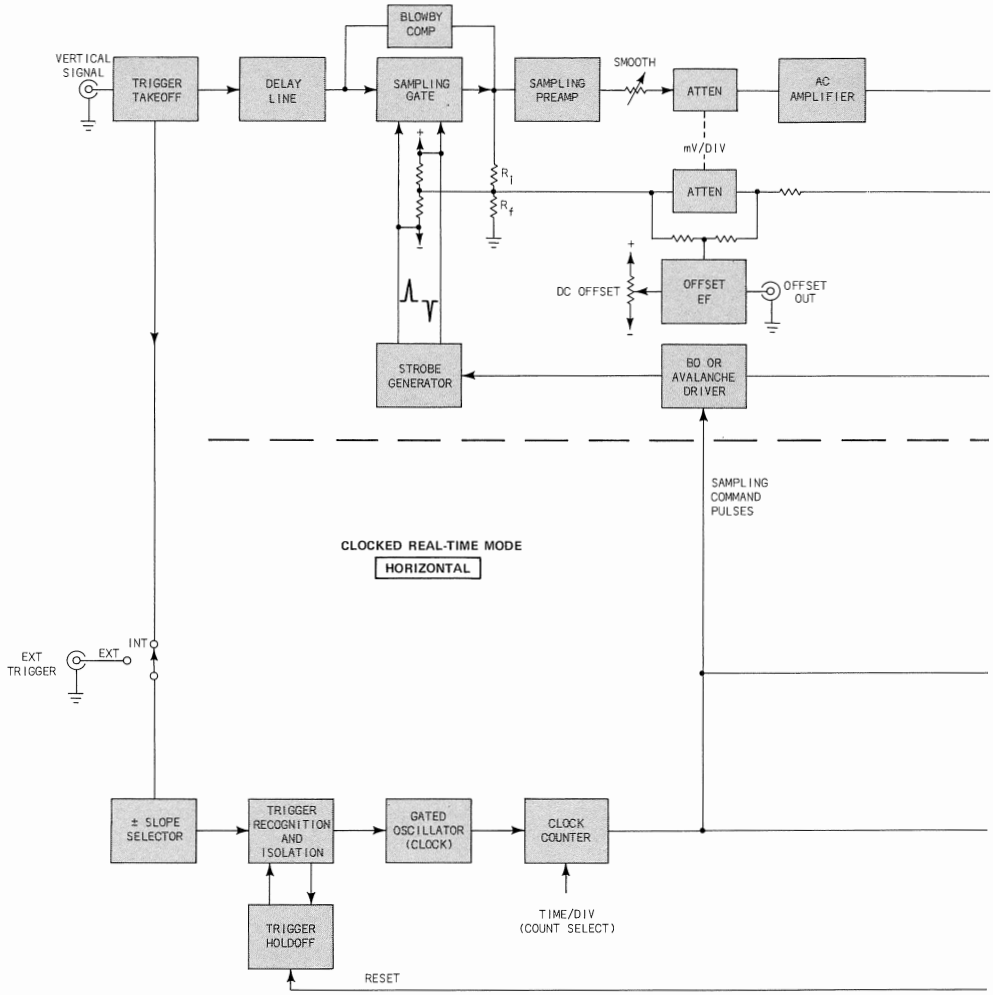


Fig. 2-8. 7T11 random mode (simplified).

The stopped level of each timing ramp is, in effect, a sample of the amplitude of the ramp at the instant it was stopped. Each stopped level is then applied to the horizontal memory and produces horizontal deflection proportional to that level for that sample. However, note that the slope of the timing ramp will be positive when started by a sampling-command pulse and will be negative when started at the instant of trigger recognition. A positive slope will normally cause the beam to be positioned to the left side of the screen and at a distance from center proportional to its stopped amplitude. A negative slope will cause the beam to be positioned to the right side of the screen at a distance proportional to its stopped amplitude. Therefore, samples of the vertical signal that are taken before the trigger-recognition points in the vertical signal will appear on-screen on the left side and samples of later points will appear on the right side.


BLOWBY COMP
VERTICAL SIGNAL
TRIGGER TAKEOFF
DELAY LINE
SAMPLING GATE
SAMPLING PREAMP
SMOOTH
ATTEN
AC AMPLIFIER
mV/DIV
ATTEN
R_i
R_f
DC OFFSET
OFFSET EF
OFFSET OUT
STROBE GENERATOR
BO OR AVALANCHE DRIVER
SAMPLING COMMAND PULSES
CLOCKED REAL-TIME MODE
HORIZONTAL
EXT TRIGGER
EXT
INT
± SLOPE SELECTOR
TRIGGER RECOGNITION AND ISOLATION
GATED OSCILLATOR (CLOCK)
CLOCK COUNTER
TRIGGER HOLDOFF
TIME/DIV (COUNT SELECT)
RESET

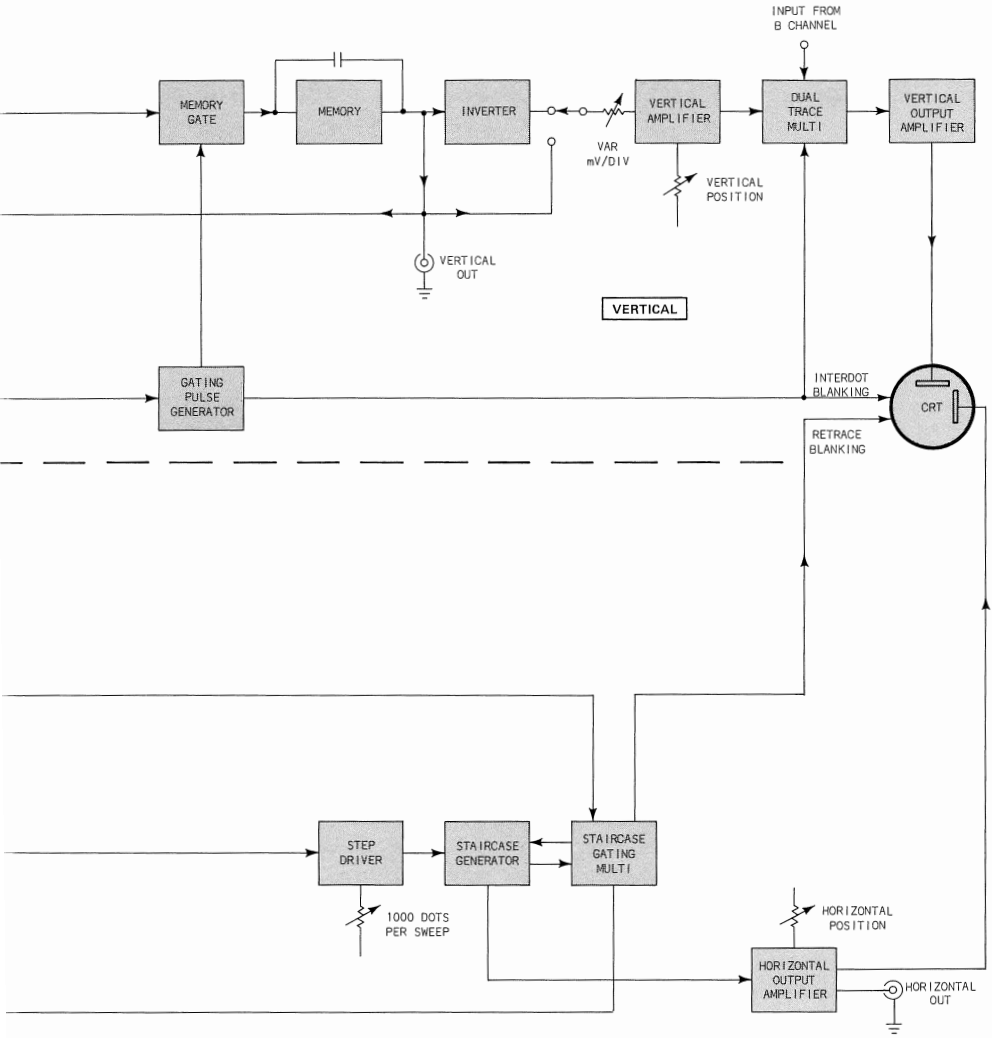


Fig. 2-9. Clocked real-time mode block diagram.

REAL-TIME MODE TIMING

Real-time sampling is used to extend the capabilities of sampling scopes so they may display slow changing voltages as well as fast changing voltages. Using the sequential mode or random mode, the time required for a complete horizontal sweep is invariably much longer than the time per division of the horizontal *scale*. The time per division of the scale is equivalent to a much shorter interval than the actual time the beam takes to traverse one division. Therefore, the sequential and random modes of sampling are sometimes referred to as equivalent-time sampling. In the real-time mode the horizontal beam velocity is the *same* as the time per division of the scale, as with conventional scopes.

There are two forms of real-time sampling. One form uses conventional-scope sweep and trigger circuits and produces a conventional sweep. With this form, the signal to be displayed is simply sampled at a high frequency that bears no synchronous relationship to the signal frequency. A free-running oscillator in the vertical section is all that is needed to generate sampling-command pulses. A conventional sweep-ramp is used for horizontal deflection and the time per division is a function of the horizontal velocity of the beam.

free-running oscillator

The other form of real-time sampling is used where digital readout is required. Refer to Fig. 2-9. This method uses a staircase sweep and the time between steps is precisely clocked. Each step in the staircase sweep corresponds to one sample of the signal, the same as for equivalent-time sampling. Unlike equivalent-time sampling, however, real-time sampling permits us to sample many points in each cycle of the signal rather than only one point per cycle.

clocked real-time sampling

In the Type 3T5 and 3T6 sampling sweep units, the real-time mode is used for time intervals of 1 ms per division and longer. At a clocked sampling rate of 100 kHz, one-hundred samples of the vertical signal are taken and displayed every centimeter when the time per division is 1 ms. At 2 ms per division, the 100-kHz clock is divided by two and signal samples are taken at a 50-kHz rate. This still provides one-hundred samples per division, a one-thousand sample

sweep and a one-thousand step staircase. The digital readout unit (6R1A or 230) measures time intervals by counting the dots between two points on the signal. A 1000-dot sweep corresponds to 100 dots per division.

By comparing block diagrams, you may see that a few circuit functions are the same in the real-time mode as in the sequential mode. One difference in the real-time mode is that the trigger-holdoff interval does not expire until a sweep is completed. In the sequential mode we trigger a fast ramp once per sample and have a trigger-holdoff function for each fast ramp. In the clocked real-time mode there are no fast ramps and we trigger only once per sweep. But there are still many samples taken each sweep.

7T11 REAL-TIME-MODE PRINCIPLES

At 50 µs/div and longer, the 7T11 switches to real-time sampling. When the real-time mode is used, sampling-command pulses are generated at a free-running average rate of 50 kHz. Timing ramps are triggered in the same way as sweep ramps are triggered in conventional oscilloscopes but the ramps don't cause any horizontal deflection. Instead, the ramps are sampled for 3 µs approximately every 20 µs. The samples are then stored in a horizontal memory and produce deflection proportional to the stored level. Each "sweep," therefore, is comprised of separate dots, each dot representing a sample of both the vertical signal and the timing ramp.

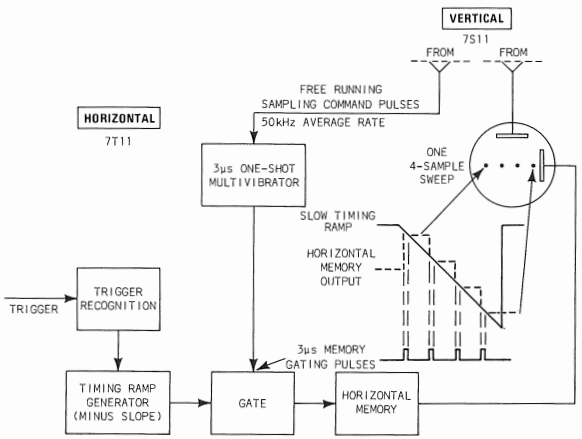


Fig. 2-10. 7T11 real-time mode (simplified).

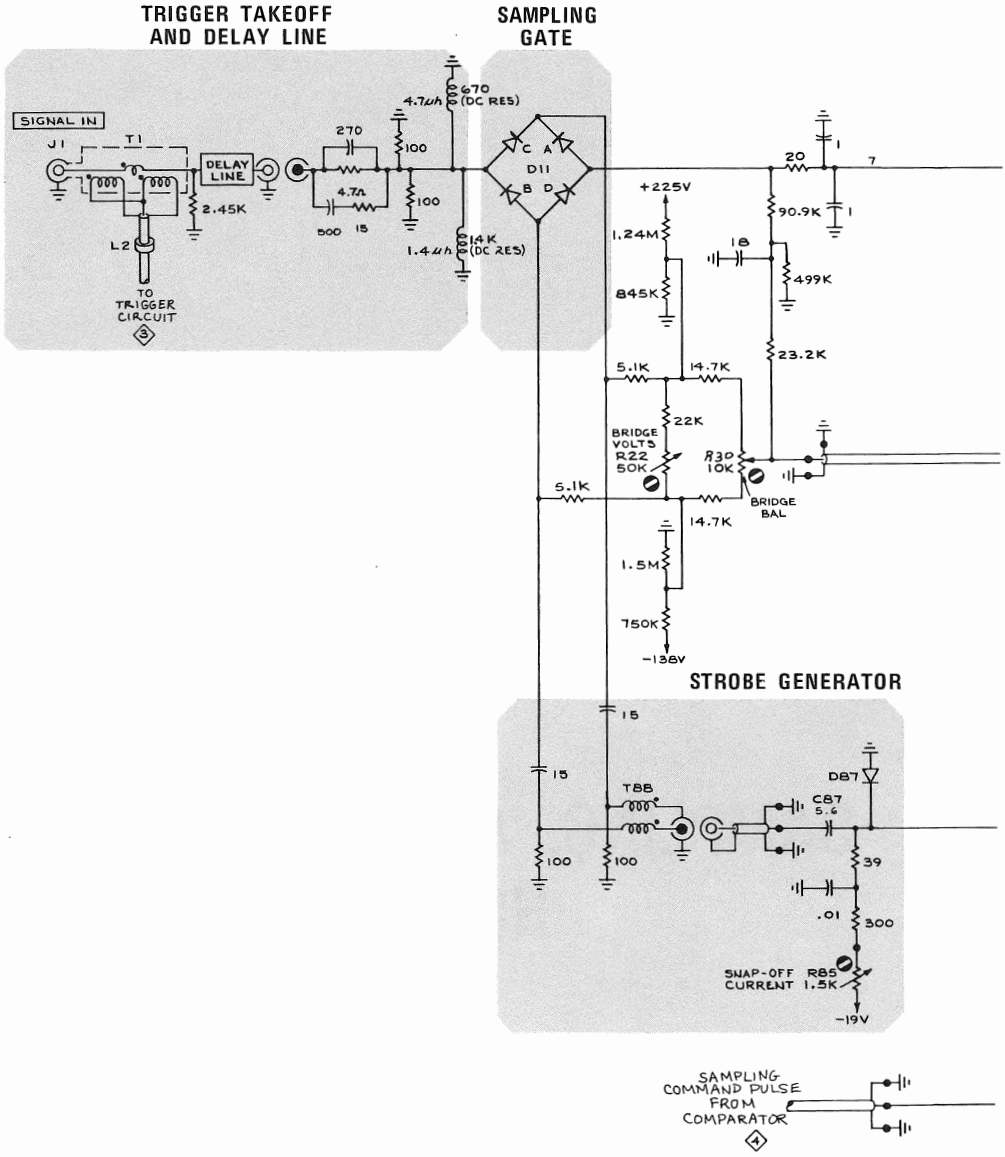
By deliberately modulating the time between samples slightly, successive sweeps invariably are comprised of dots in different horizontal positions so that wide gaps between dots do not appear to be present.

Each sample of the vertical signal is taken at the *beginning* of the 3-µs wide ramp gating pulses. And each sample of a timing ramp corresponds to the level at the end of the 3-µs gating pulses. So, a sample of the vertical signal that precedes the beginning of a timing ramp by no more than 3 µs can be displayed along with samples that are taken while a ramp is running. Three microseconds of lead time may, therefore, be displayed.

Also, time position (delay) of at least one screen width is available the same as with sequential sampling or random sampling.

3

SAMPLING, AMPLIFYING AND HOLDING CIRCUITS


TRIGGER TAKEOFF AND DELAY LINE
SAMPLING GATE
SIGNAL IN
J1
T1
DELAY LINE
2.45K
L2
TO TRIGGER CIRCUIT
3
270
4.7Ω
500
15
100
100
4.7μh
670 (DC RES)
1.4μh
14K (DC RES)
D11
C
A
B
D
+225V
1.24M
845K
5.1K
14.7K
22K
BRIDGE VOLTS R22 50K
R30 10K
BRIDGE BAL
5.1K
14.7K
1.5M
750K
-138V
20
1
7
90.9K
1
18
499K
23.2K
STROBE GENERATOR
15
15
T88
D87
C87 5.6
100
100
39
.01
300
SWAP-OFF CURRENT
R85 1.5K
-19V
SAMPLING COMMAND PULSE FROM COMPARATOR
4

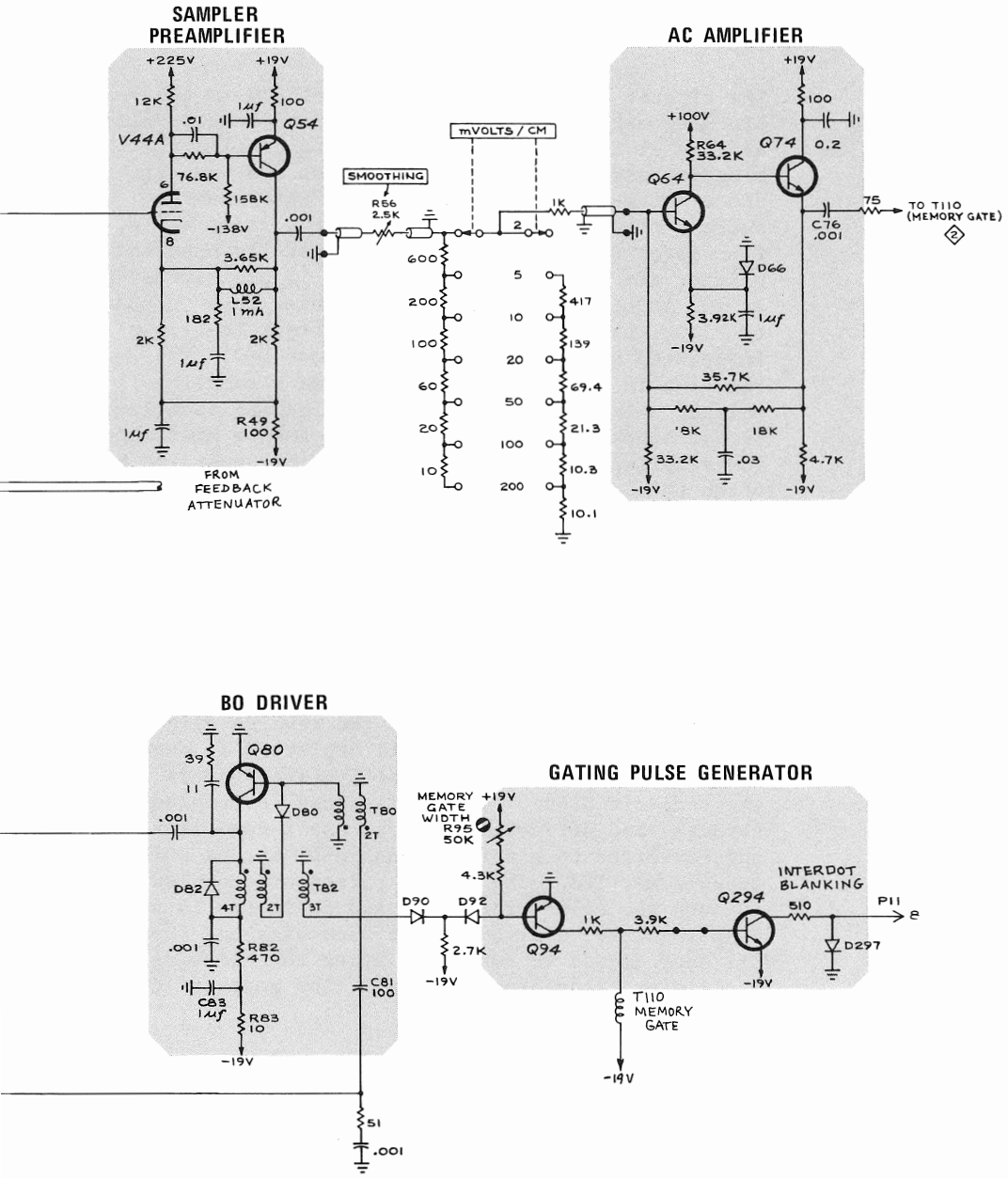


Fig. 3-1. 1S1 Sampler.

1S1 SAMPLER CIRCUITS

BLOCKING OSCILLATOR DRIVER

The circuit involving the transistor Q80 is the blocking oscillator. When a sampling-command pulse arrives at the input to the blocking oscillator, the blocking oscillator fires and drives the snap-off diode (step-recovery diode) D87 so that reverse current flows through the diode for a short while. Transistor Q80 is usually off because its base and emitter are at the same potential. A positive step at the input to transformer T80 causes base current to flow, which causes collector current to flow, increasing base current through diode D80. The reaction is regenerative. Each time a sampling-command pulse is introduced, the blocking oscillator fires, blocks and recovers in less than a microsecond. The sampling-command pulses may not be generated more often than about every ten microseconds.

STROBE GENERATOR

Each time the blocking oscillator transistor Q80 conducts, its collector goes up, diverts the forward current from snap-off diode D87 and reverses the direction of current flow through the snap-off diode. Until the current carriers that were mobilized in the snap-off diode, due to forward conduction, have a chance to turn around and recross the diode junction, the diode conducts heavily in the reverse direction. When the supply of carriers is depleted, it happens suddenly and a very steep positive step occurs across the snap-off diode. This pulse edge is coupled through, and differentiated by, small capacitor C87 and converted to a pair of push-pull strobe pulses by transformer T88. The strobe pulses are coupled through the 15-pF capacitors and delivered to the sampling gate, overcoming the back bias and causing all four diodes to conduct. After the blocking oscillator transistor turns off, the snap-off diode becomes forward biased again.

The forward current through the snap-off diode is adjusted with R85, the Snap-off Current potentiometer. Snap-off current is adjustable to accommodate the individual differences between snap-off diodes to minimize risetime to the specified amount while keeping random noise to a minimum.

GATING-PULSE GENERATOR

The function of the gating-pulse generator circuit is to generate pulses which will: (1) admit the amplified, sampled signal to the memory at the right moments for an appropriate interval of time and (2) blank the CRT beam while it would be moving. Both transistors, Q94 and Q294, are usually off. A negative-going drive pulse from the blocking oscillator interrupts the current that was flowing through D90. That turns on Q94. The resulting collector current pulse in the primary winding of T110 gates the memory and admits any amplified sample. The base of Q294 is returned to the same level as its emitter through the 3.9-k resistor and the primary winding of T110. When Q94 turns on and a voltage is developed across that winding, Q294 conducts and blanks the CRT beam.

Potentiometer R95 adjusts the width of the memory gating pulse by affecting how hard Q94 is driven into saturation. The drive pulse that turns Q94 on does not last as long as the transistor conducts. The memory gating pulse width is normally adjusted to maximize the sampling-loop gain. That happens when the memory capacitor has all the time necessary to charge or discharge to a new level but not so much time that the new level changes. The coupling time-constant of the amplifier stages is fairly short, causing a step signal to eventually be differentiated and the memory capacitor to change its charge if gated on too long.

TRIGGER TAKEOFF

The trigger takeoff circuit in the 1S1 consists of a small transformer T1, located in the coaxial environment next to the vertical signal input connector on the front panel. The secondary of the transformer has considerably more turns than the primary so the takeoff voltage, which is developed across 50 ohms via a 50-ohm cable, reflects only a small resistance in series with the input. To minimize reflections from the small apparent increase in input impedance at this point, the 2.45-k resistor is placed in shunt with the input. This makes the input at the front panel look like 50 ohms instead of a somewhat higher resistance. If the cable which delivers the pickoff signal is not loaded in precisely 50 ohms, some input energy is reflected and

appears as an aberration in the display. Furthermore, fast pulse edges in the trigger-recognition circuits are not completely isolated, so are coupled back from the collector of the isolation transistor in the trigger circuits and introduce low millivolt aberrations in the display, following the trigger-recognition point.

Although the trigger-takeoff transformer provides a voltage step-up, only about ten percent of the input voltage is delivered as a triggering signal. That amounts to about one percent of the energy of the input signal.

delay line

The delay line in the 1S1 consists of a specially constructed 50-ohm coaxial cable having a delay of about 40 nanoseconds. The top-corner rounding of a positive step signal introduced by this delay line is considerable. See Fig. 2-2. The network of resistors, capacitors and inductors, between the end of the delay line and the sampling gate, provide approximate compensation for the rounding. A small increase in forward gain of the following amplifiers is required and that causes a small degradation in the signal-to-noise ratio in the display.

SAMPLING GATE

The 1S1 sampling gate consists of four matched Shottky-barrier diodes D11A, D11B, D11C, D11D. These diodes are back biased all the time except for the very brief moments when push-pull strobe pulses are coupled through the two 15-pF capacitors in series with the leads that come from the strobe generator. Unless the input signal is too high in amplitude, the diodes block conduction of the input signal beyond the gate except when the strobe pulses are present. The strobe pulses overcome the back bias and make all four diodes conduct. The amount of back bias is equal to the voltage-drop across the two series resistors comprised of the adjustable Bridge Volts control, R22, and the adjacent 22-k resistor. The voltage-drop is produced by an essentially constant current dependent on the value of the resistors that connect to the -138 volt supply and to the +225 volt supply. The wiper arm of the Bridge Balance pot, R30, is a relatively low-impedance point because it is connected to the output of the feedback attenuator. The voltage at the wiper arm is determined by what is fed back, and although the voltage at that point does not effect the corner-to-corner bridge voltage, it

does determine how much bias exists across each diode with respect to ground and the input signal.

When the diodes in the sampling gate are turned on by the strobe pulses, the signal voltage existing at the input to the sampling gate at that moment causes current to pass into or out of the sampling preamplifier through the sampling gate diodes. When signal current is passing through the gate, the total current through two opposite diodes, such as D11A and D11B, increases while the total current through the other pair decreases.

SAMPLING PREAMP

The 1S1 sampling preamplifier consists of the circuits involving vacuum tube V44A and transistor Q54. The *signal* input to this preamplifier is the output of the sampling gate, always a step-signal when there is a difference in voltage across the gate and always having a risetime practically equal to the time the sampling gate admits the input signal. The other input to the sampling preamplifier comes from the feedback attenuator and offset circuits via the 23.2-k and 90.9-k resistors. The preamp is designed for low noise, medium bandwidth and constant gain. The cathode of V44A and the collector of Q54 are at the same DC potential, being practically shorted together by the inductor L52. V44A and Q54 share a constant current in such a way as to hold the plate voltage of V44A nearly constant. That means the current through both V44A and Q54 are nearly constant and signal gain is, therefore, essentially constant.

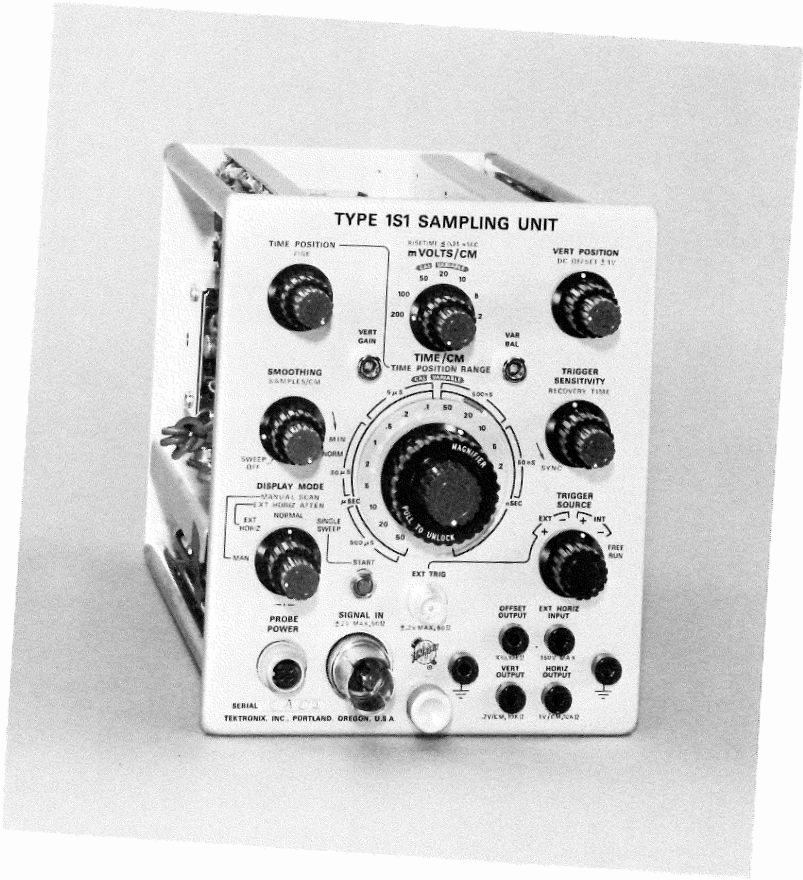
Although the signal this preamp responds to is a step signal with a risetime of approximately 350 picoseconds, the forward gain amplifiers have about 1000 times that long to amplify the step while the amplified version is stored in the memory capacitor. They don't need to have a very fast response time.

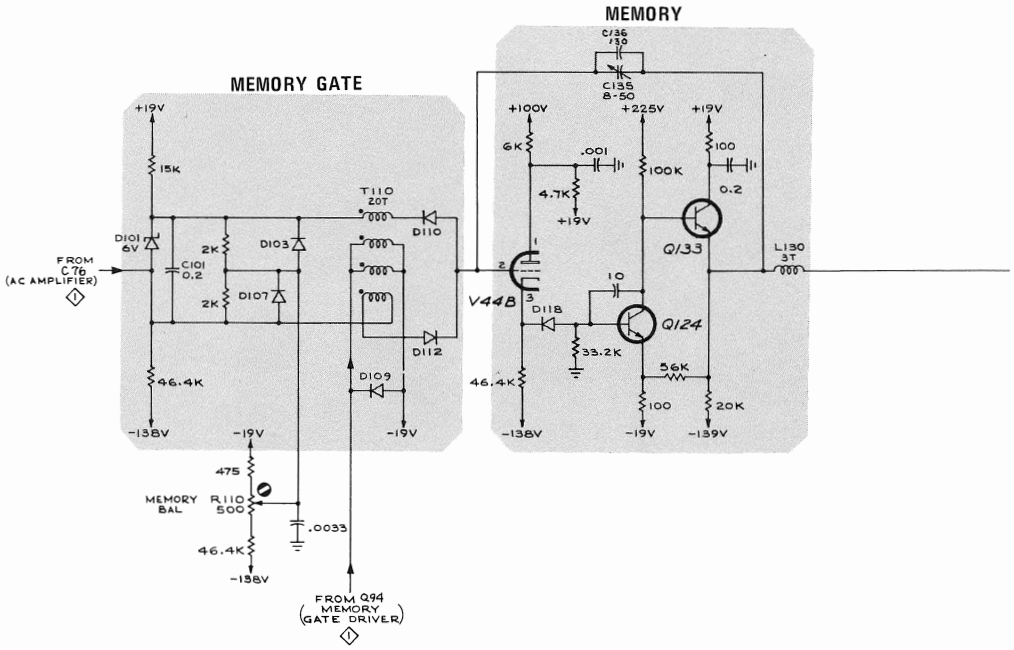
FORWARD GAIN ATTENUATOR

The forward gain attenuator reduces the forward gain by a factor as great as 100 to 1 in a 1-2-5 sequence. It is designed to provide a practically constant load for the output of the preamp stage as well as a nearly constant source impedance for driving the next amplifier stage. The SMOOTHING control, R56, provides additional attenuation of forward gain when it is desirable to reduce random noise or time-jitter in the display.

AC AMPLIFIER

The AC amplifier involves transistors Q64 and Q74, a fedback pair similar to an operational amplifier. Q74 acts like an emitter follower. The high open-loop voltage gain of Q64 and the fixed ratio of input resistance to feedback resistance assures constant gain. The resistor in the emitter circuit of Q64 should pass more current than required in the collector circuit to drop the collector voltage the necessary amount to operate the base of Q74 below its collector voltage. The additional current flows through diode D66 holding the emitter slightly below ground. The emitter is well by-passed by the 1-μF capacitor across the diode. The emitter of emitter-follower Q74 should operate about halfway between ground and the +19 volts on its collector, depending on what level is required to raise the base level of Q64 close to ground, determined by the divider action of the 35.7-k resistor and the 33.2-k resistor.


TYPE 1S1 SAMPLING UNIT
TIME POSITION
mVOLTS/CM
VERT POSITION
VERT GAIN
VAR BAL
TIME/CM
TIME POSITION RANGE
SMOOTHING
TRIGGER SENSITIVITY
MAGNIFIER
PULL TO UNLOCK
DISPLAY MODE
TRIGGER SOURCE
EXT TRIG
PROBE POWER
SIGNAL IN
OFFSET OUTPUT
EXT HORIZ INPUT
VERT OUTPUT
HORIZ OUTPUT
TEKTRONIX, INC., PORTLAND, OREGON, U.S.A.


MEMORY
MEMORY GATE
C136
#30
C135
8-50
+19V
15K
T110
20T
D110
D101
6V
2K
D103
FROM
C76
(AC AMPLIFIER)
C101
0.2
2K
D107
D112
46.4K
D109
-138V
-19V
-19V
475
MEMORY
BAL
R110
500
.0033
46.4K
-138V
FROM Q94
MEMORY
(GATE DRIVER)
+100V
+225V
+19V
6K
.001
100K
100
4.7K
+19V
0.2
Q133
L130
3T
V44B
1
2
3
10
D118
Q124
33.2K
46.4K
56K
100
20K
-138V
-19V
-139V

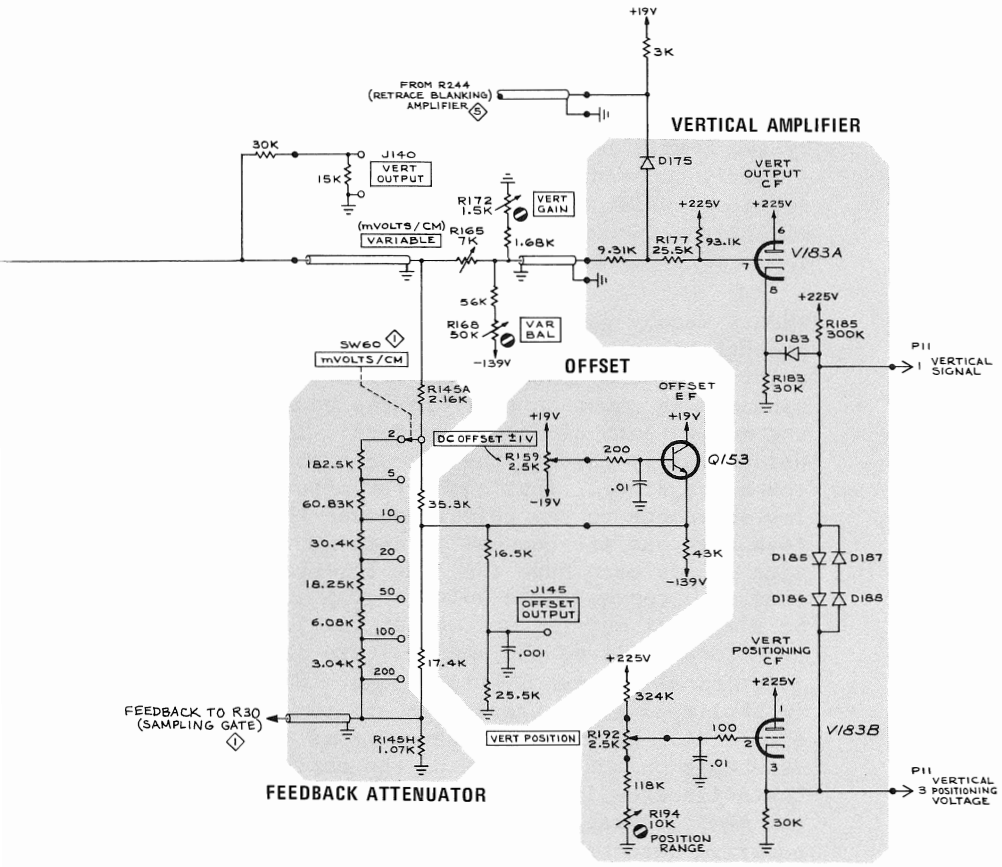


Fig. 3-2. 1S1 Memory.

1S1 MEMORY CIRCUITS

MEMORY GATE

Like a sampling gate circuit, the memory gate circuit consists of some back biased diodes that are turned on for brief moments when it is desirable to pass a signal. Diodes D110 and D112 are the memory gate diodes. Diodes D103 and D107 are also back biased by the same voltage that back biases the memory gate diodes but they perform only an incidental function, that of occasionally clipping excessively large amplified signals. The back-bias voltage is developed by the 6-volt zener diode D101 which is in series with a fairly constant current supply. The two 2-k resistors which shunt the zener diode have their midpoint returned to an adjustable voltage by R110, the Memory Bal pot.

When a memory gating current pulse is delivered through the center windings of transformer T110, the polarity of the voltage induced in the secondary windings is right to overcome the back bias and cause the memory gate diodes to conduct. The diode current passes mostly through the 0.2-μF capacitor that shunts the zener diode. That capacitor offers only a very low impedance to the pulses because they are typically less than one microsecond in duration. If the memory gate diodes each have the same forward resistance when they conduct, the voltage drop across each will be identical and the voltage at the junction of the two diodes will be the same voltage as exists at the junction of the two 2-k resistors. Whenever there is an amplified input signal, one of the sampling gate diodes will be turned on harder than the other depending on the polarity of the amplified signal. The difference in current then charges or discharges the memory capacitors (C135 and C136) either in the positive direction or the negative direction. When the memory gating pulse ends and the memory gate diodes are again back biased, the memory capacitors have a very high-impedance path through which to charge or discharge. It therefore takes a long time to do so. The memory gate diodes must have very low leakage and low storage.

MEMORY

When no input signal (and zero offset voltage) is present, the output side of the memory capacitor should ideally be at zero volts if the memory is being gated rapidly. It inevitably drifts away from

that voltage when not gated. If gated very slowly, the drift can be viewed as vertical "dot slash," where each dot starts to drift but is restored to its correct vertical position with each new gating pulse. The drift is perceived as an error signal at the input to the sampling preamplifier and the sampling loop nulls the error with each sample.

The memory consists of a DC-coupled inverting amplifier with high open-loop gain. The memory capacitor connects the output back to the input, attempting to keep the voltage at the input constant. The voltage on the center arm of the Memory Bal pot R110 is slightly below -19 volts and this voltage is practically the same voltage that appears on the grid of V44B when gated. When properly adjusted, that voltage is what is required to set the output of the DC-coupled amplifier close to zero volts. The output voltage is not *measured* when making this adjustment, however. A simpler method is to vary sampling-loop gain with the SMOOTHING control and set R110 to minimize a vertical shift in the trace.

VERTICAL AMPLIFIER

In the Type 1S1 the vertical amplifier provides no gain. It's main purpose is to DC-couple the output of the memory from a zero-volt reference level to a reference level of about +67.5 volts, the level required at the deflection amplifiers at the input to the oscilloscope mainframe. The signal at the output of the memory is actually attenuated by the resistors between the output of the memory and the grid of vacuum tube V183A. The amount of attenuation is adjustable with R165, the front panel VARIABLE gain control. When the VARIABLE control is in the calibrated position, the attenuation is set with R172, the VERT GAIN potentiometer, so that the right amount of deflection is produced in the oscilloscope when a known voltage is applied to the input of the sampling unit. When the output from the memory is zero volts, the VAR BAL pot R168 is set so the current through the grid voltage-divider resistors is right to prevent the trace from moving vertically when the VARIABLE control is rotated.

During retrace intervals, when diode D175 conducts, it is the same as applying a large negative signal to the amplifier; the beam is deflected off-screen downward. The rest of the time the diode is back biased.

Only cathode follower V183A delivers a signal to the scope mainframe. V183B is a cathode follower that is used to set the nominal +67.5 volt level on the other input to the scope mainframe so the trace may be near center screen when no signal is applied and when the vertical position control is near center. To prevent overdriving the amplifier stages in the mainframe, the diodes between the two cathodes of the cathode followers limit the difference in cathode voltage to about 1 volt. Diodes D185, D186, D187 and D188 do not conduct except when the grid voltages of the cathode followers differ by nearly 1 volt.

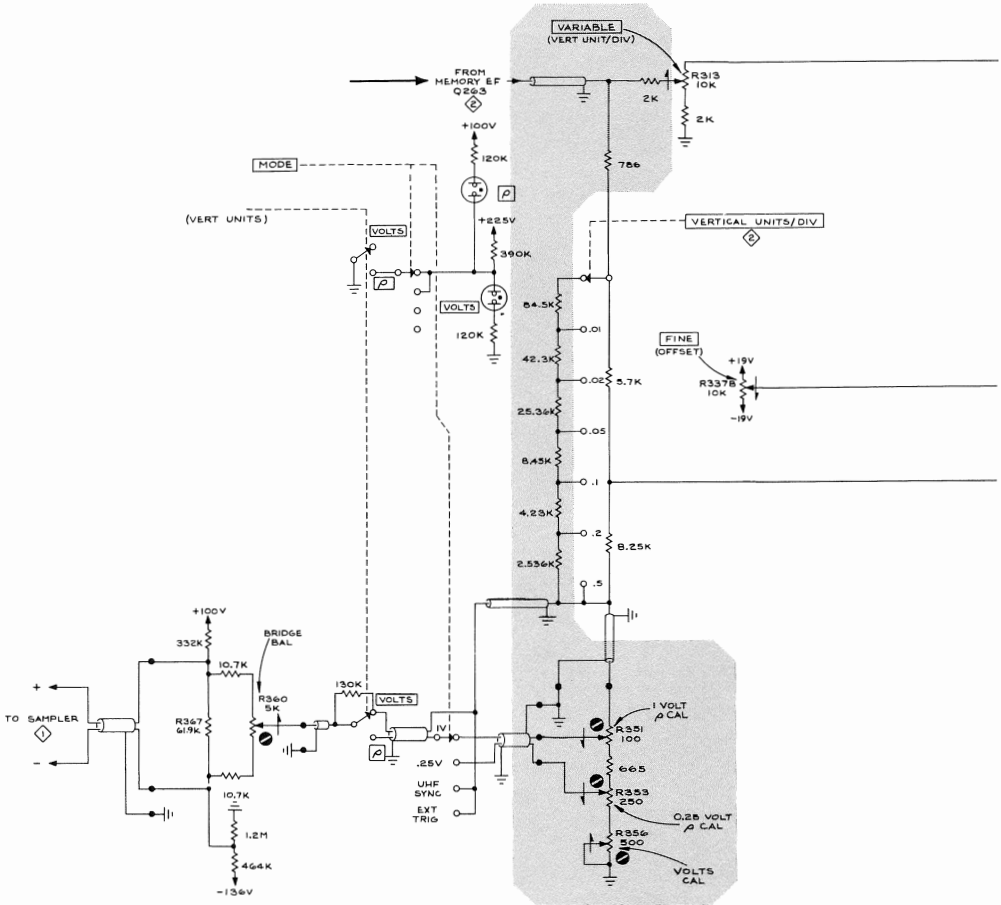
OFFSET

The emitter of emitter follower Q153 varies from about -19 volts to about +19 volts when the DC OFFSET control is rotated through its range. The offset voltage which gets fed back to the input of the sampling preamplifier is the voltage developed across resistor R145H by the current flowing through the 17.4-k resistor connected to the emitter follower. A little more than ±1 volt may be fed back. The offset voltage may be monitored at the OFFSET OUTPUT jack, which has a source resistance of 10 kilohms. If measured with a nonloading meter, the offset voltage is ten times the amount of voltage fed back.

FEEDBACK ATTENUATOR

At a sensitivity of 200 mV/div the feedback attenuator consists of precision resistor R145A in series with precision resistor R145H. At all other sensitivities at least one other precision resistor is inserted between those two to provide additional feedback attenuation. At 200 mV/div the feedback signal is attenuated by a factor of 3 to 1. At that sensitivity a 200-mV signal at the input should produce 600 mV (3 x 200) at the output of the memory. At 100 mV/div the attenuation is 6 to 1 so a 100-mV signal at the input should produce 600 mV at the output of the memory; and so on.


TYPE 1S2 SAMPLING UNIT
OFFSET
VERTICAL UNITS/DIV
POSITION
RESOLUTION
NORMAL
HIGH
VERT GAIN
DISPLAY MODE
NORMAL
MAN
SINGLE SWEEP
EXT HORIZ
INPUT
START
VOLTS
HORIZONTAL UNITS/DIV
DISTANCE
TIME
RANGE
DIELECTRIC
MAGNIFIER
EXT TRIG INPUT
MODE
THRU SIGNAL CHANNEL 50Ω
PULSE SOURCE 50Ω
INT PULSE
EXT TRIG
UHF SYNC
VERT OUTPUT
HORIZ OUTPUT
SERIAL
TEKTRONIX, INC. PORTLAND, OREGON U.S.A.



FEEDBACK ATTENUATOR

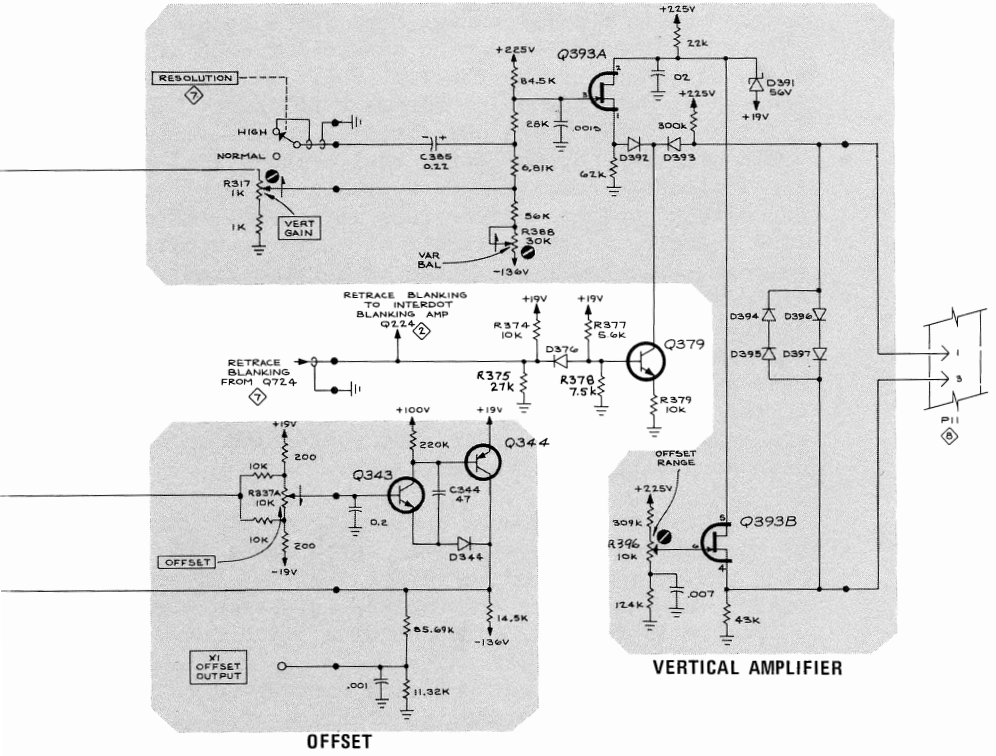


Fig. 3-3. 1S2 Offset and Output Stage.

1S2 OFFSET AND OUTPUT STAGE CIRCUITS

FEEDBACK ATTENUATOR

The feedback attenuator in the 1S2 is very similar to the one in the 1S1 except that three possible values of attenuation may be chosen for each of the seven positions of the VERTICAL UNITS/DIV switch instead of just one value for each position. In the 1S2 the vertical units per division may be either VOLTS or ρ (the Greek letter rho). The symbol stands for reflection coefficient, a term which applies to the size of voltage reflections in a transmission line relative to the original or incident applied voltage. The numerical value of a reflection expressed in ρ units tells us what decimal fraction of the applied incident voltage was reflected. For example, a reflection having a value of 0.1 ρ would have a voltage amplitude equal to 10% of the value of the incident applied step voltage. Displayed at a sensitivity of 0.1 ρ/div, the reflection should have an amplitude of one division.

Feedback attenuation must correspond to the value of the incident step signal if reflections from the step are to correspond to vertical divisions of the scale. Because there are two separate step signals available in the 1S2, each having a different amplitude, two separate adjustments are available to make the feedback attenuation correspond to the step being used. The amplitude of one step signal is approximately one volt. Potentiometer R351 (1 Volt ρ Cal) is used to adjust feedback attenuation so that signal and its reflections are displayed at their correct amplitude. The other step signal is about 0.25 volts in amplitude. The 0.25 Volt ρ Cal pot R353 is used to display that signal and its reflections at their correct amplitude. The total value of R351, R352, R353 and R356 is adjusted with R356, the Volts Cal potentiometer, so that feedback attenuation may be set to display voltage at the right amplitude. That control should be set first because it affects the other control settings.

OFFSET

The offset circuit is very similar to that in the Type 1S1 except there are two offset controls (coarse OFFSET and FINE) and the offset drive, instead of being from an emitter follower, is from a temperature-stabilized signal-follower transistor pair, Q343 and Q344.

There is no front panel vertical positioning control on the 1S2. Positioning is done with the offset controls. That way, whenever a signal is on the screen, the offset voltage fed back to the sampling gate is optimum to keep the sampling gate operating in the middle of its dynamic range. Larger signal voltages may be handled this way. Without a front panel position control, however, the vertical position of a zero volt input level using zero volts of offset may not be in the center of the screen unless the deflection amplifiers in the scope mainframe are perfectly balanced. To center a zero volt, zero offset trace, an internal screwdriver adjustment, Offset Range, is provided in the vertical amplifier circuit.

VERTICAL AMPLIFIER

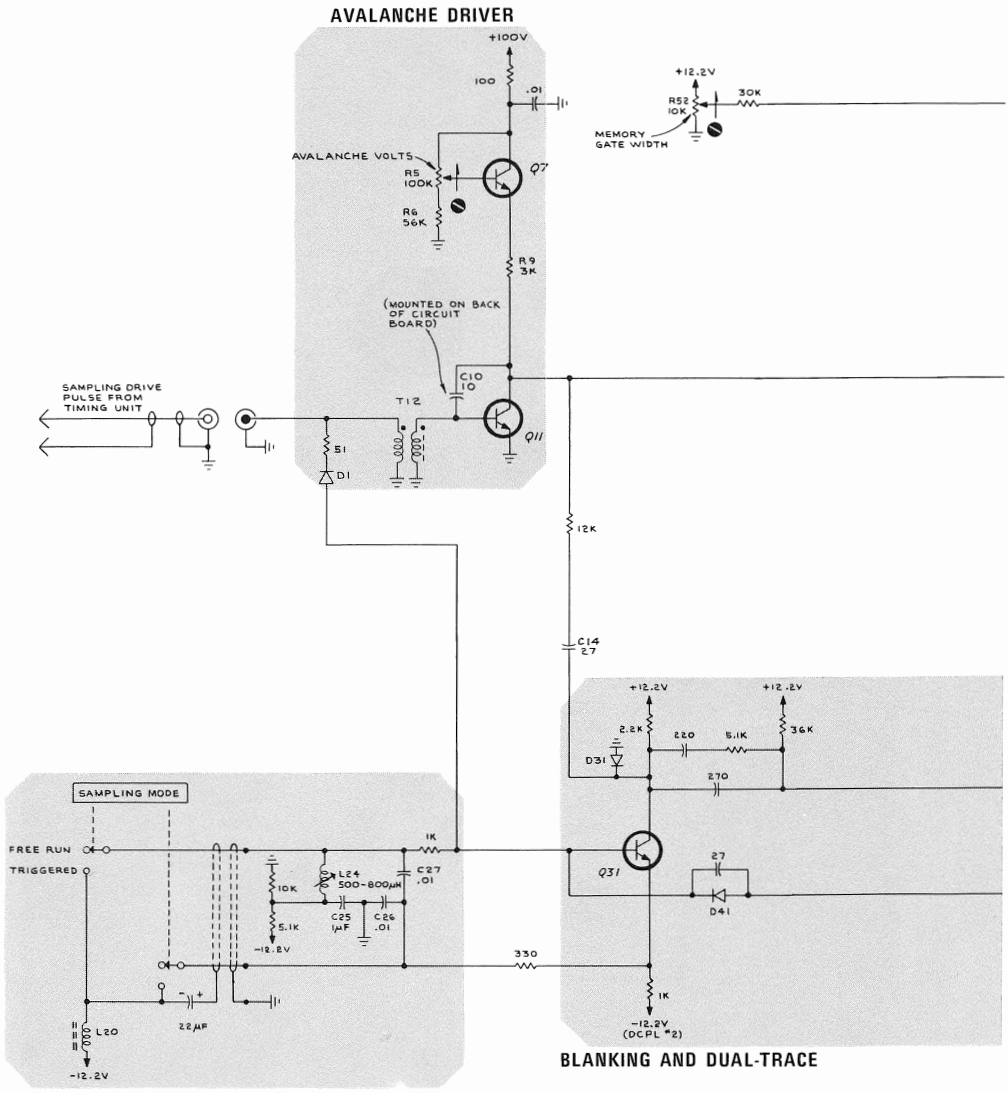
The Offset Range pot, R396, sets the voltage level at the gate terminal of source follower, Q393B, to a nominal +67.5 volts to match the output level of signal source follower, Q393A, to produce a centered trace when zero volts is applied at the output of the memory circuit. The potentiometer may be adjusted to compensate for several divisions of deflection amplifier imbalance in the scope mainframe in which the 1S2 is used, instead of adjusting or repairing the scope amplifier.

The output signal from the memory circuit is delivered to the gate terminal of FET Q393A. The signal goes through the front panel VARIABLE UNITS/DIV control, R313, and the front panel screwdriver adjustment VERT GAIN control, R317. It then goes through the string of voltage-divider resistors that elevate the gate terminal of FET Q393A to about +67.5 volts and attenuate the signal 5X.

Notice the 0.0015-μF capacitor at the gate terminal of FET Q393A. The function of this capacitor is to integrate the memory output signal slightly before delivering it to the deflection amplifiers in the scope mainframe. This reduces random noise in the display. Random noise is further reduced when the HIGH RESOLUTION mode is selected, by connecting a larger 0.22-μF capacitor to ground. That capacitor is connected to the junction of the 28-k and 6.8-k resistors in the divider string.

Source follower Q393A is usually connected to the output line that goes to the deflection amplifiers because diodes D392 and D393 both normally conduct. Transistor Q379 operates as a constant-current transistor with the current determined by the base voltage and by the value of its emitter resistor. The base voltage is usually about +10 volts so the emitter current is about 1 mA. About 0.5 mA flows through diode D392 and the 300-k resistor and the remainder flows through FET Q393A. During retrace intervals, the base level of Q379 goes close to ground, reducing its emitter and collector current below 0.5 mA, shutting off current through diode D392 and allowing the output line to rise considerably above the level of the other deflection amplifier output lead. One pair of diodes, D394 and D395 or D396 and D397, conduct and prevent the deflection amplifiers from being overdriven when one output line tries to differ in voltage from the other by more than about 1 volt.


TYPE 3S1 DUAL-TRACE SAMPLING UNIT
A POSITION
B POSITION
RISETIME ≤ 0.35 ns
DUAL-TRACE
SMOOTH
NORMAL
CHAN A
CHAN B
A+B
mVOLTS/DIV
mVOLTS/DIV
50
20
10
100
5
200
2
A VERT
B HORIZ
POSITION
A DOT RESPONSE
VERT GAIN
B DOT RESPONSE
INVERT
NORM
INVERT
NORM
A INPUT
± 2V MAX, 50Ω
INTERNAL TRIGGER
SAMPLING MODE
FREE RUN
OFF
TRIGGERED
A
B
B INPUT
± 2V MAX, 50Ω
PROBE
PROBE
A OFFSET B
OUT
A OUT
B OUT
SERIAL
TEKTRONIX
PORTLAND, OREGON U.S.A.


AVALANCHE DRIVER
+100V
100
.01
AVALANCHE VOLTS
R5
100K
Q7
R6
56K
R9
3K
(MOUNTED ON BACK OF CIRCUIT BOARD)
C10
10
T12
Q11
SAMPLING DRIVE PULSE FROM TIMING UNIT
51
D1
+12.2V
R52
10K
30K
MEMORY GATE WIDTH
12K
C14
27
+12.2V
+12.2V
2.2K
220
5.1K
36K
D31
270
Q31
27
D41
SAMPLING MODE
FREE RUN
TRIGGERED
1K
10K
L24
500-800μH
C27
.01
C25
1μF
C26
.01
5.1K
-12.2V
330
1K
-12.2V
(DCPL #2)
L20
22μF
-12.2V
100 kHz OSCILLATOR/REAL TIME
SAMPLING COMMAND PULSE GENERATOR
BLANKING AND DUAL-TRACE

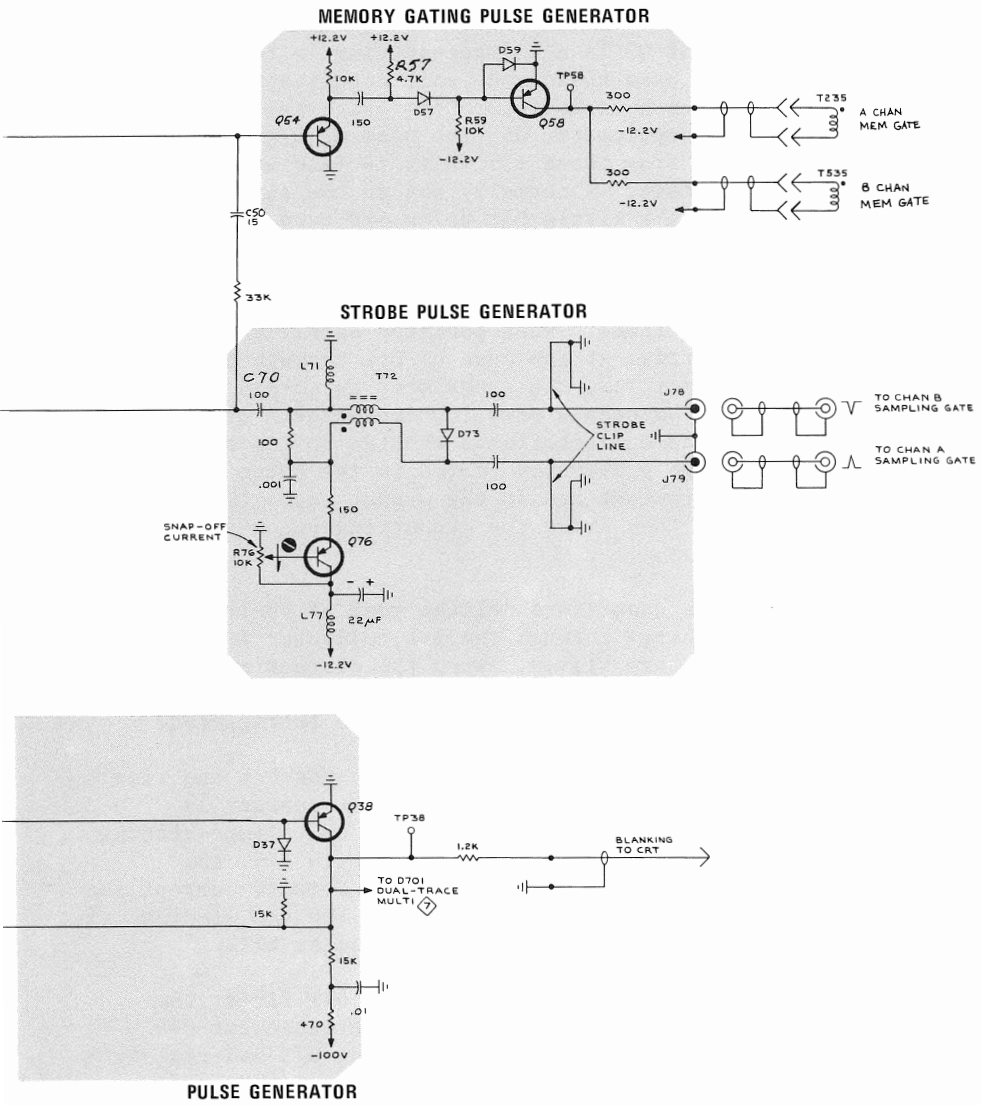


Fig. 3-4. 3S1 Gate Generators.

3S1 GATE GENERATORS CIRCUITS

AVALANCHE DRIVER

Transistor Q7 is a voltage-setting emitter follower used to set the collector supply voltage for avalanche transistor Q11. With the Avalanche Volts potentiometer R5, the base of Q7 may be set anywhere from about +35 volts to +100 volts. The potentiometer is normally set so the supply voltage for Q11 is a little bit below its zero bias collector breakdown voltage. Above that voltage the transistor becomes a sustained negative-resistance oscillator and generates strobe pulses at the wrong times. When positive sampling-command pulses arrive at the base of Q11 through pulse transformer T12, the transistor is turned on and suddenly becomes a very low impedance. It acts as though its collector were shorted to its emitter. The charge previously stored in the three small capacitors that are in the output leads (C50, C70 and C14) then drive the connecting pulse-generator circuits.

After the capacitors deliver most of their charge, they recharge through the 3-k collector load of the avalanche transistor. When the current stops, the transistor collector voltage goes up to the emitter level of Q7 and Q11 is ready to be retriggered.

STROBE PULSE GENERATOR

Diode D73 is the snap-off diode. Most of the time it passes a forward current. That current is dependent on the emitter voltage of voltage-setting emitter follower Q76 and is set with R76, the Snap-off Current potentiometer. Forward current for the snap-off diode flows through the two windings of transformer T72, and through inductor L71.

When avalanche-driver transistor Q11 fires, the high-voltage charge in the 100-pF capacitor C70 reverses the current through diode D73 and rapidly sweeps out all its carriers. Because the same reverse current flows in opposite directions through the windings of transformer T72, it appears to have essentially no inductance. When the current carriers in the snap-off diode suddenly disappear, a steep voltage wavefront is delivered through the two 100-pF capacitors to Channel A and Channel B sampling gates. The step signal is converted to narrow strobe pulses by the clip lines.

BLANKING AND DUAL-TRACE PULSE GENERATOR

This circuit is essentially the same as in the 3S5. See that circuit description for details (page 82).

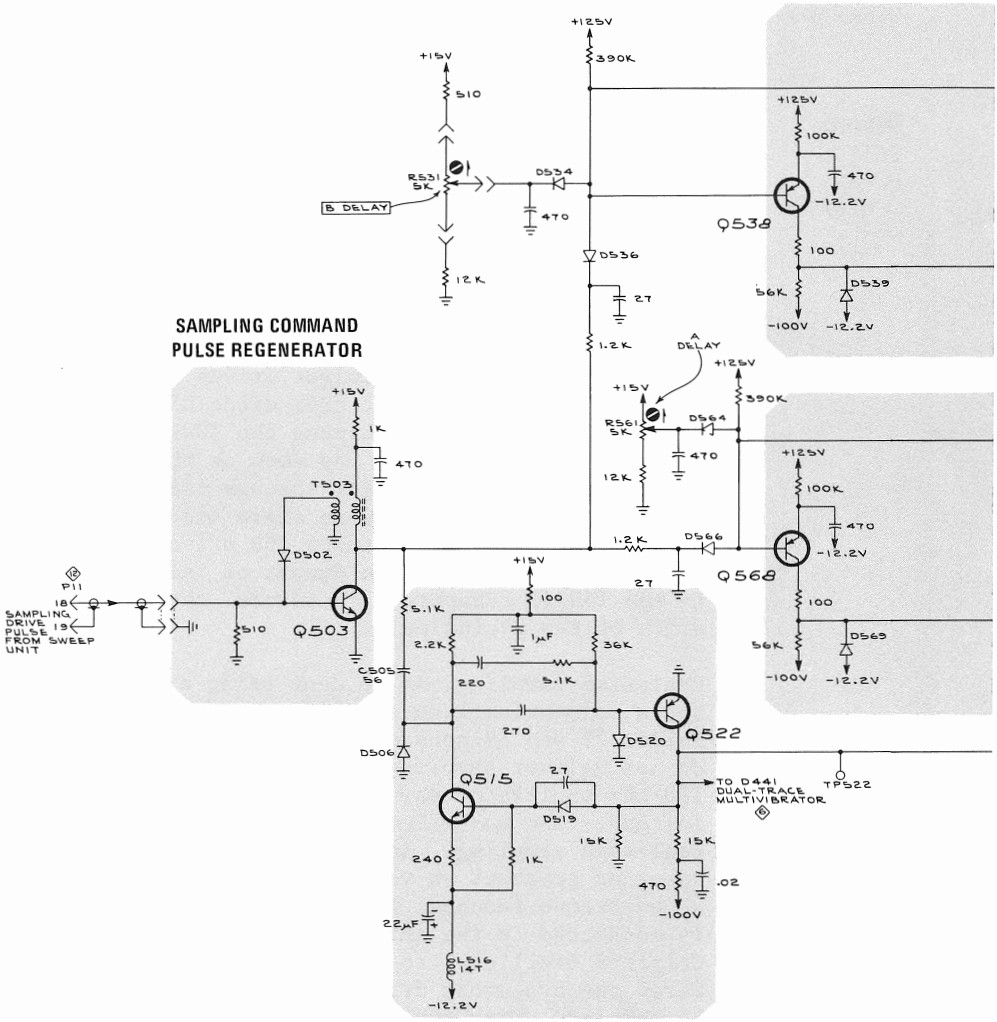
MEMORY GATING PULSE GENERATOR

Transistor Q54 is usually on and transistor Q58 is usually held off by current flowing through diodes D59, D57 and resistor R57. The 150-pF capacitor in the emitter circuit of Q54 will have a charge of about 1 to 11 volts depending on the emitter level of Q54, which depends on the setting of the Memory Gate Width potentiometer, R52. When the avalanche driver delivers a tall negative-going pulse, transistor Q54 saturates for a period longer than needed for a memory gating pulse. When Q54 saturates and its emitter drops to ground level, the charge in the 150-pF capacitor drives diode D57 below ground, diverting current from diode D59 and permitting the current through the 10-k base circuit resistor to turn on Q58. As soon as the 150-pF capacitor loses its charge, through the 4.7-k resistor, diode D57 turns on again and diverts base current from Q58. That turns Q58 off and ends the memory gating pulse. The amount of initial charge in the 150-pF capacitor, therefore, determines the width of the gating pulse.

100-kHz OSCILLATOR

REAL-TIME SAMPLING

Real-time sampling may be done using a 3S1 plug-in and a conventional nonsampling time-base plug-in unit. Series 2B and 3B nonsampling time-base plug-in units do not deliver sampling-command pulses, so the 100-kHz oscillator may be used to generate them instead. The so-called FREE-RUN mode is used for real-time sampling. In that mode the base of Q31 is returned to about -8 volts, turning it on. Regenerative feedback from the 330-ohm resistor that is connected to the emitter of Q31 causes the Colpitts oscillator to run continually. Every cycle fires the avalanche driver and causes the signal to be sampled. When switched to the other mode, the base of Q31 is returned to -12.2 volts, the same level as the emitter supply, keeping Q31 normally turned off.


SAMPLING COMMAND
PULSE REGENERATOR
BLANKING AND DUAL-TRACE
DRIVE PULSE GENERATOR
+125V
390K
+15V
510
R531
5K
B DELAY
D534
470
12K
D536
27
1.2K
A
DELAY
R561
5K
D564
470
12K
1.2K
D566
27
+125V
100K
470
-12.2V
Q538
100
56K
D539
-100V
-12.2V
Q568
D569
+15V
1K
470
T503
D502
P11
18
SAMPLING
DRIVE
PULSE
19
FROM SWEEP
UNIT
510
Q503
5.1K
100
1μF
2.2K
36K
220
5.1K
C505
56
270
D506
Q515
27
D519
Q522
D520
TO D441
DUAL-TRACE
MULTIVIBRATOR
6
TP522
15K
15K
240
1K
470
.02
-100V
22μF
+
-
6L516
214T
-12.2V

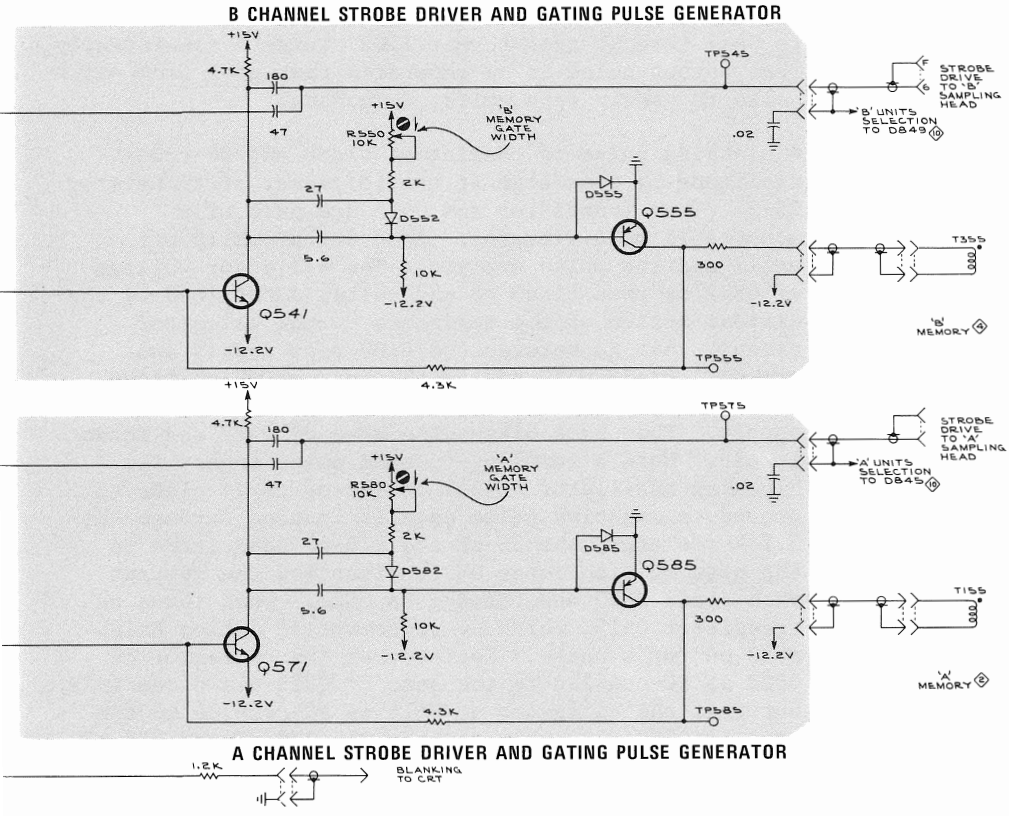


Fig. 3-5. 3S5 Gate Generators.

3S5 GATE GENERATORS CIRCUITS

SAMPLING-COMMAND PULSE REGENERATOR

A blocking oscillator regenerates the incoming sampling-command pulses. Transistor Q503 is normally off but is turned on by the first rising portion of the input pulse. Regenerative feedback from collector to base through transformer T503 causes a consistently fast output pulse to be generated that goes from +15 volts to nearly zero volts, then back.

BLANKING AND DUAL-TRACE DRIVE PULSE GENERATOR

A blanking pulse of consistent width and 50-volts amplitude is generated at the collector of transistor Q522. That transistor and Q515 are part of a monostable multivibrator. Both are normally off until a drive pulse arrives. The collector voltage of Q522 is then close to -50 volts, determined by the divider action of the resistors in the collector circuit that go between the -100 volt supply and ground. Diode D520 passes the current which flows through the 36-k resistor connected to the +15 volt supply. That back biases the base of Q522 and turns it off. When a sampling-command pulse causes the blocking oscillator (Q503) collector to go close to ground, a negative pulse edge is coupled through the 5.1-k resistor, the 56-pF and 270-pF capacitors to the base of transistor Q522, diverting the current from diode D520 and turning on Q522. That turns on transistor Q515, which by regenerative action holds Q522 on for a while. Notice that the collector of Q522 is DC-coupled to the base of Q515 via diode D519 but that the collector of Q515 is AC-coupled to the base of Q522. As soon as both the 270-pF and 220-pF capacitors at the collector of Q515 are charged, the base current of Q522 stops flowing and the two transistors cut off. The duration of the pulse is largely determined by the time constant of the 220-pF capacitor and the 5.1-k resistor in series with it.

STROBE DRIVER AND GATING PULSE GENERATOR

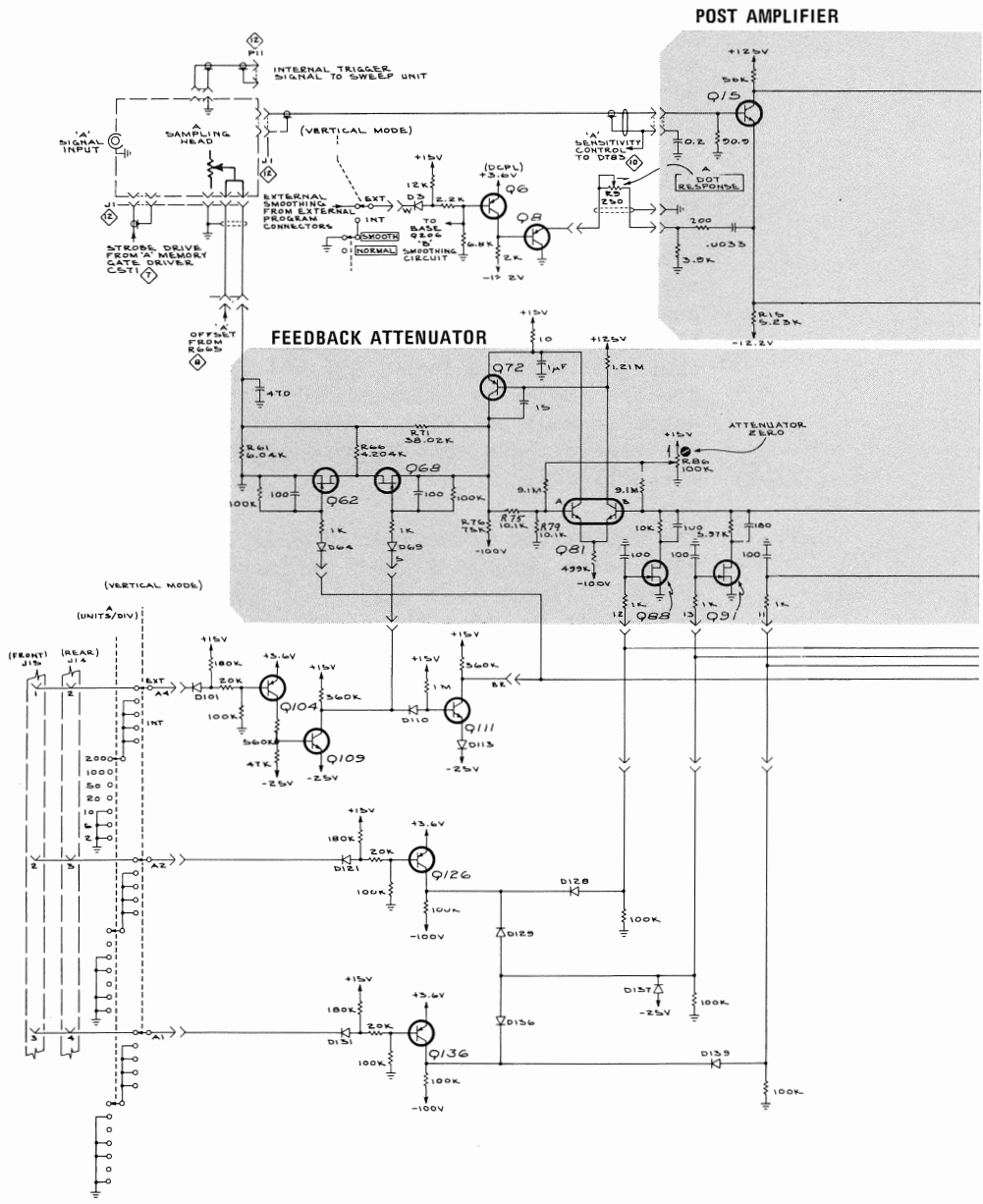
Both the A channel and B channel circuits are identical in operation, so only the B channel (top) circuit will be discussed. The 3S5 must produce two independent strobe generator drive signals so that the times when two sampling heads sample may be adjusted to be coincident. (Dual-trace instruments that have only one strobe generator circuit to generate two pairs of push-pull strobe pulses don't need to be adjusted. But then any difference in delay in the delivery of the strobe pulses has to be carefully controlled and two signals that do *not* occur simultaneously may not be sampled and compared as closely.)

To make it possible to delay the display on either channel with respect to the other, both are delayed and the delay of one channel (channel B) is made adjustable from the front panel. The front panel B DELAY range is about 10 ns so the internal adjustment for A Delay, R561, is normally set to the middle of the range, about 5 ns.

Delay is introduced by simultaneously generating two fast down-going ramps across two 27-pF capacitors each time the collector of the blocking oscillator transistor Q503 goes to ground. The two capacitors are the ones which join the two 1.2-k resistors that connect to the collector of Q503. They are normally charged to +15 volts and run down until the diodes that join them conduct. The voltage at which the diodes conduct is independently set by the delay controls R531 and R561. These controls determine the resting base voltage of transistors Q538 and Q568 respectively.

The emitter of transistor Q538 is longtailed to +100 volts through a 100-k resistor so normally passes slightly less than 1 mA. That current is not sufficient to cause the necessary voltage drop (88 volts) across the 56-k collector resistor, so diode D539 conducts and back biases the base of transistor Q541, holding it off. Diodes D552 and D555 normally conduct also and keep Q555 turned off. When the ramp voltage at the cathode end of diode D536 goes lower than the base voltage of transistor Q538, the diode conducts and turns on Q538. Transistor Q541 then turns on quickly and delivers a strobe generator drive pulse through the 180-pF capacitor to the B channel sampling head.

The negative output step is also fed back through the 47-pF capacitor to the base of Q538 helping it turn on very quickly. When the collector of Q541 goes down, it turns on Q555 via the 5.6-pF capacitor. When Q555 is on, it keeps Q541 on. When the collector of Q541 goes below the emitter level of Q555 (ground), Q555 is kept turned on by base current which passes through the 10-k resistor that is returned to -12.2 volts. When the 27-pF capacitor charges sufficiently, diode D552 will conduct again. The time the capacitor takes to charge is partly determined by the B Memory Gate Width control, R550. That control is normally set to maximize sampling-loop gain.


POST AMPLIFIER
FEEDBACK ATTENUATOR
INTERNAL TRIGGER SIGNAL TO SWEEP UNIT
'A' SIGNAL INPUT
'A' SAMPLING HEAD
(VERTICAL MODE)
'A' SENSITIVITY CONTROL TO DT85
DOT RESPONSE
EXTERNAL SMOOTHING FROM EXTERNAL PROGRAM CONNECTORS
EXT
INT
SMOOTH
NORMAL
TO BASE Q206 'B' SMOOTHING CIRCUIT
(DCPL) +3.6V
STROBE DRIVE FROM 'A' MEMORY GATE DRIVER CS71
'A' OFFSET FROM R693
ATTENUATOR ZERO
(VERTICAL MODE)
(UNITS/DIV)
(FRONT) J15
(REAR) J14
Q15
Q72
Q68
Q62
Q81
Q88
Q91
Q104
Q109
Q111
Q126
Q136
+12.5V
+15V
-12.2V
-100V
-25V
+3.6V

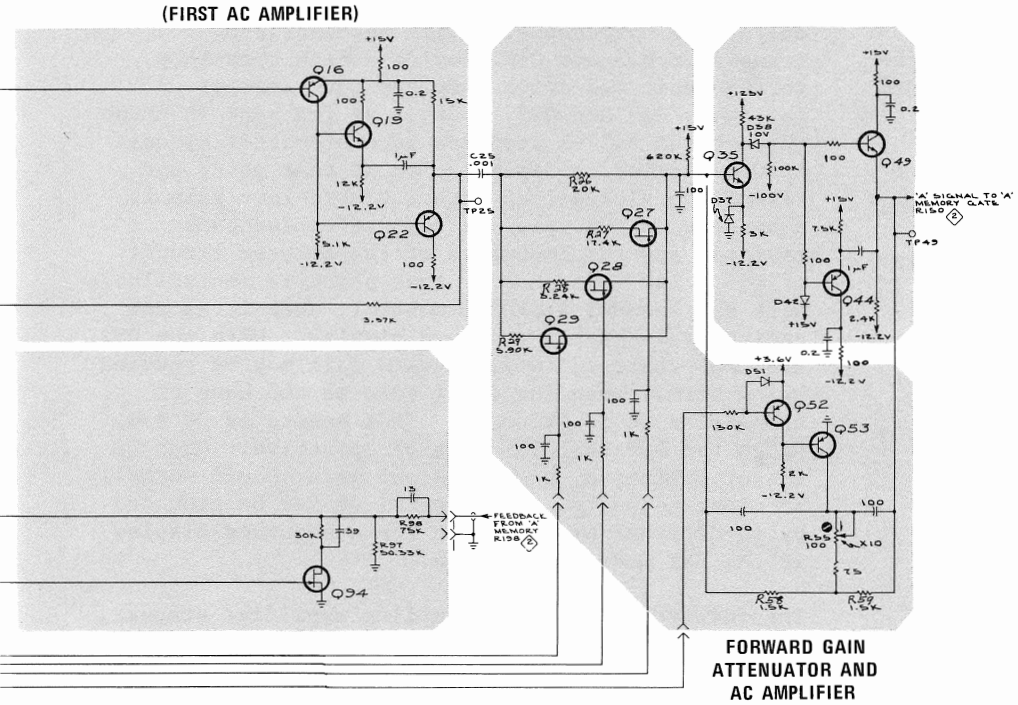


Fig. 3-6. 3S5 Ch A Programmed Amp and Attenuators.

3S5 CH A PROGRAMMED AMP AND ATTENUATORS CIRCUITS

POST AMPLIFIER (FIRST AC AMP)

Both channel A and channel B circuits are alike so only those for channel A will be described. Transistor Q15 and Q16 provide a high open-loop voltage gain and drive complementary emitter followers Q19 and Q22. Output is fed back in phase through the 3.57-k resistor to the emitter circuit of Q15 increasing degeneration at that point and fixing the closed-loop gain. Closed-loop gain is dependent on the value of the 3.57-k feedback resistor and the impedance of the emitter circuit of Q15. The impedance at that point is controllable with R9, the DOT RESPONSE control, when it is not desirable to have a smoothed display. With the DOT RESPONSE control, total forward gain may be reduced below normal when the input line to the base of transistor Q6 is grounded. That saturates Q8 and makes the DOT RESPONSE control operative. When Q8 is not operative, sampling-loop gain should normally be close to unity. The base of Q6 may be grounded by an external program line for a smoothed display if the EXT mode is selected.

FORWARD-GAIN ATTENUATOR AND AC AMPLIFIER

The forward gain of the sampling amplifier stages is determined by what sensitivity is selected. There are seven choices -- either 2, 5, 10, 20, 50, 100 or 200 units/div. When selecting sensitivity, either from the front panel or by remote program, some combination of input lines A1, A2 and A4 are grounded.

Resistor R26 is the input resistor to the second AC amplifier, an operational amplifier, with R58 and R59 in series in the feedback path. Field effect transistors Q27, Q28 and Q29 shunt the input resistor when they are turned on and are practically an open circuit when off. Turning on any one or a combination of these FET's increases forward gain. The forward gain also may be increased by reducing the feedback from the output of the operational amplifier. That is done when Q53 is turned on hard, practically grounding its collector, making a 10-to-1 divider out of R59, R56 and R55. An extra forward gain of 10X is therefore provided by turning on Q53. That happens whenever the A4 line is grounded because transistor Q111 is turned off, which turns off Q52 and turns on Q53.

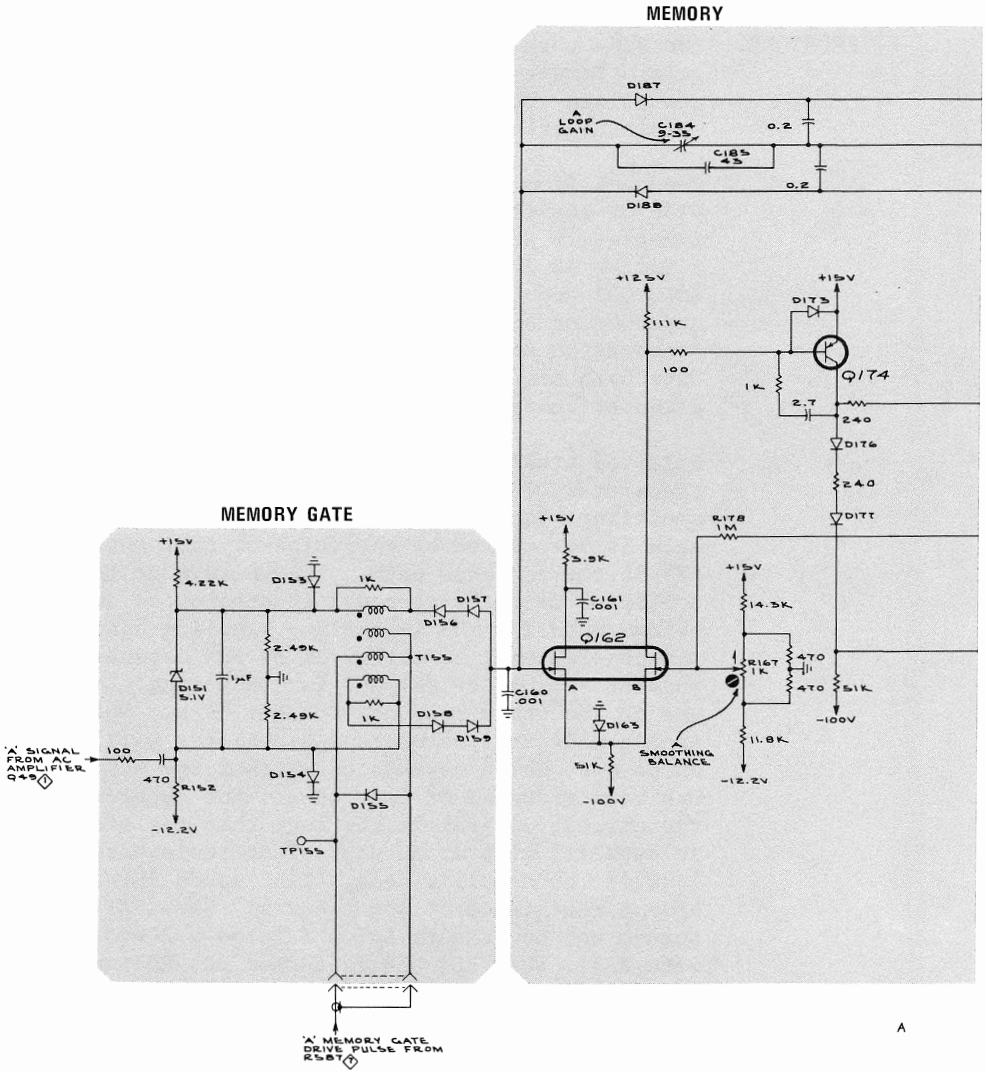
FEEDBACK ATTENUATORS

Feedback attenuation is controlled by grounding the same three input lines used to control forward gain. Forward gain and feedback attenuation are controlled together so sampling-loop gain may remain constant.

Feedback from the memory enters the right-hand side of the feedback attenuation circuit and is immediately attenuated by resistors R98 and R97 by a factor of 2.5 to 1. If field effect transistors Q88, Q91 and Q94 are all turned off, no further attenuation occurs at that point. Further attenuation does occur when Q88 or Q94 is turned on. When both are turned on, Q91 is also turned on and attenuation is greatest at that point.

Balanced transistor Q81, in conjunction with transistor Q72, form a noninverting DC-coupled fedback amplifier with a precise voltage gain of two. The gain is determined by the value of resistors R75 and R79 in the feedback path. The voltage at the collector of transistor Q72 is attenuated once more before entering the (S-series) sampling head. The attenuation will be either 2X or 20X depending on whether FET Q62 or FET Q68 is conducting. Normally one or the other conducts but not both. Which one conducts depends on whether transistor Q111 is turned on or off, which depends on whether the input line A4 has been grounded or left open. Not apparent from the circuit diagram is the fact that resistor R61 has in parallel with it an equivalent resistance of about 14 k in the sampling head. That makes R61 appear to have a resistance of about 4.2 k. When FET Q62 is turned on, R66 shunts R61 and forms a 20-to-1 divider with R71. When FET Q68 is turned on, R66 shunts R71 and forms a 2-to-1 divider across R61.

The Attenuator Zero pot R86 adjusts the 2X amplifier so that zero volts at the input will produce zero volts at the output.


MEMORY
MEMORY GATE
D187
LOOP GAIN
C184 9-35
0.2
C185 43
0.2
D188
+12.5V
+15V
111K
100
D173
Q174
1K
2.7
240
D176
240
D177
2178 1M
+15V
3.3K
C161 .001
Q162
+15V
14.3K
R167 1K
470
470
51K
-100V
11.8K
SMOOTHING BALANCE
-12.2V
C160 .001
D163
51K
-100V
+15V
4.22K
D153
1K
D157
D156
2.49K
T155
D151 5.1V
1μF
2.49K
1K
D158
D159
'A' SIGNAL FROM AC AMPLIFIER Q49
100
470
R152
-12.2V
D154
D155
TP155
'A' MEMORY GATE DRIVE PULSE FROM RS87
A

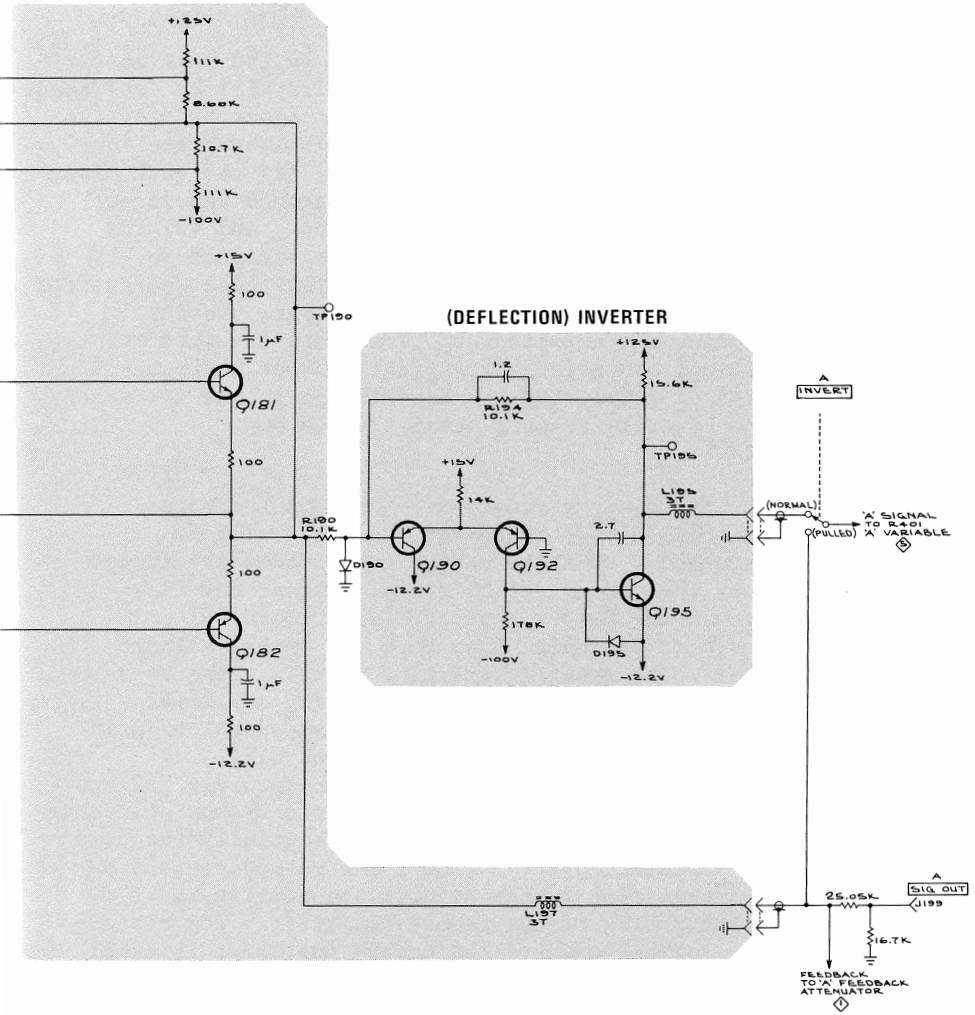


Fig. 3-7. 3S5 Ch A Memory.

3S5 CHANNEL A MEMORY CIRCUITS

MEMORY GATE

The 3S5 memory gate for channel B is the same as for channel A so only channel A circuits will be described. Operation is very much the same as described for the 1S1. The main differences are: (1) there are four memory-gate diodes instead of two, (2) the back bias is equal amounts above and below ground and is not adjustable with a memory balance pot, and (3) the bridge turn-on transformer T155 is designed to minimize capacitively coupled gating pulse energy from being coupled to the memory amplifier, thereby reducing the amplitude of transients fed into the vertical amplifier and digital readout instruments (6R1A or 230). See the description of the 1S1 memory gate circuit for more details (page 66).

MEMORY

The 3S5 memory circuits are the same for both channels so only those for channel A will be discussed. When the memory gate diodes are turned on by the memory gating pulse, current may flow through the memory capacitor(s) (C184-C185) and charge or discharge them to a new output voltage level. The input to FET Q162 is held close to zero volts by feedback from the inverting amplifier through the memory capacitor. High open-loop gain is provided by transistors Q162 and Q174. Transistors Q181 and Q182 are complementary NPN and PNP emitter followers jointly driven by the collector circuit of Q174. They provide essentially the same low-impedance drive for up-going output signals as for down-going output signals, equalizing the response time of the memory amplifier. The closed-loop voltage gain of the memory amplifier is equal to the ratio of the value of the 470-pF capacitor at the input to the memory gate and the value of the memory capacitor in the feedback path.

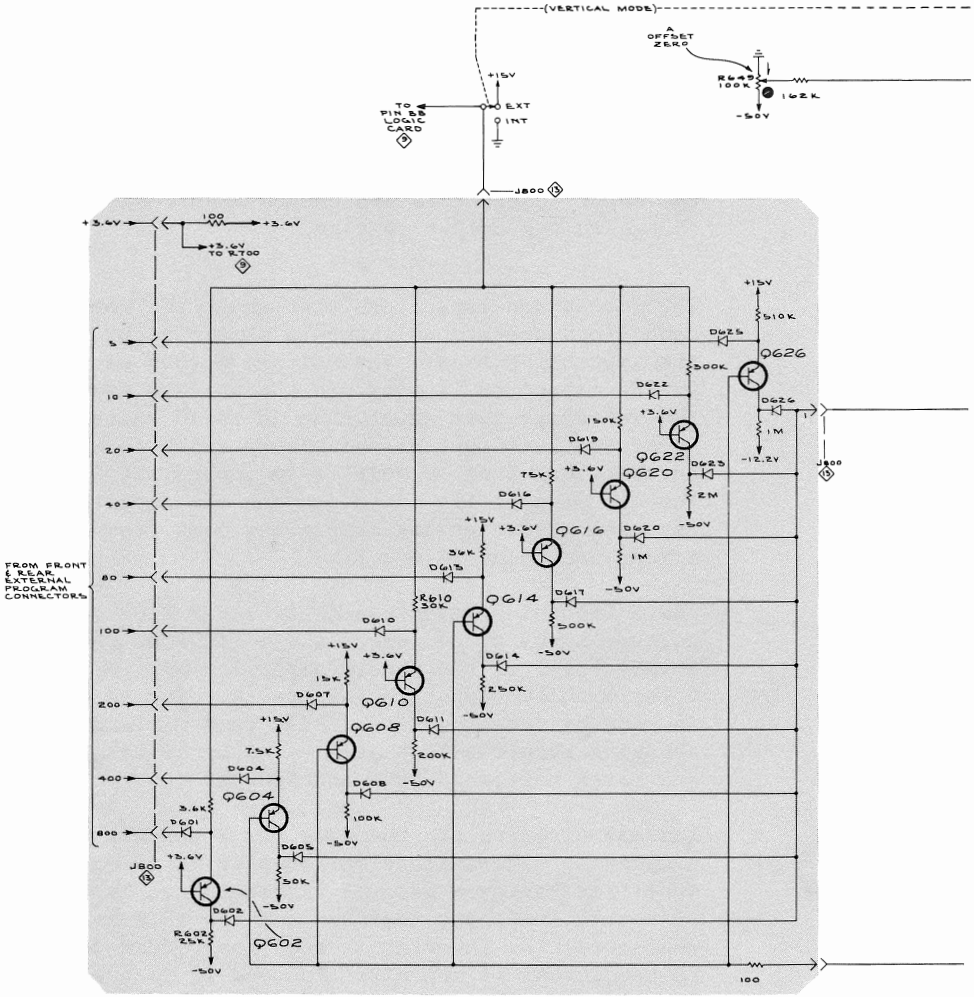
The .001-μF capacitor to ground at the input to the gate terminal of FET Q162 provides temporary storage for current passing through the memory gate, reducing the requirements for a wideband memory amplifier. In other words, any charge temporarily stored in the .001-μF capacitor during the short time when the memory gating pulse admits an amplified, sampled signal is shortly thereafter transferred to the memory capacitors and causes a corresponding change in the output voltage.

The diodes and capacitors that shunt the memory capacitors operate only when a sample might drive the spot off-screen. The voltage across each 0.2-μF capacitor is equal to the voltage drop across the resistors that shunt them (8 to 10 volts) and whenever the output of the memory tries to swing further than 8 or 10 volts from ground, it is clamped. The clamping action is to prevent the amplifiers from saturating so that any sample may come from an off-screen condition in one try.

The A Smoothing Balance potentiometer R167 sets the voltage level at the gate of FET Q162B so that the output level of the memory amplifier will be zero volts when the input is zero volts. The adjustment is made by reducing trace shift to a minimum while changing sampling-loop gain -- as by switching back and forth between SMOOTH and NORMAL.

DEFLECTION INVERTER

The 3S5 circuits are the same for B channel as for A channel. The deflection inverter is an operational amplifier having a gain of 1X determined by the ratio of the 10.1-k input resistor and the 10.1-k feedback resistor. The inverter is used to produce deflection in the normal (+ up) direction and it is bypassed when it is desirable to have a positive-going signal produce down-going deflection. The common-emitter balanced input stage helps make the output independent of temperature changes.



OFFSET CURRENT SELECTOR

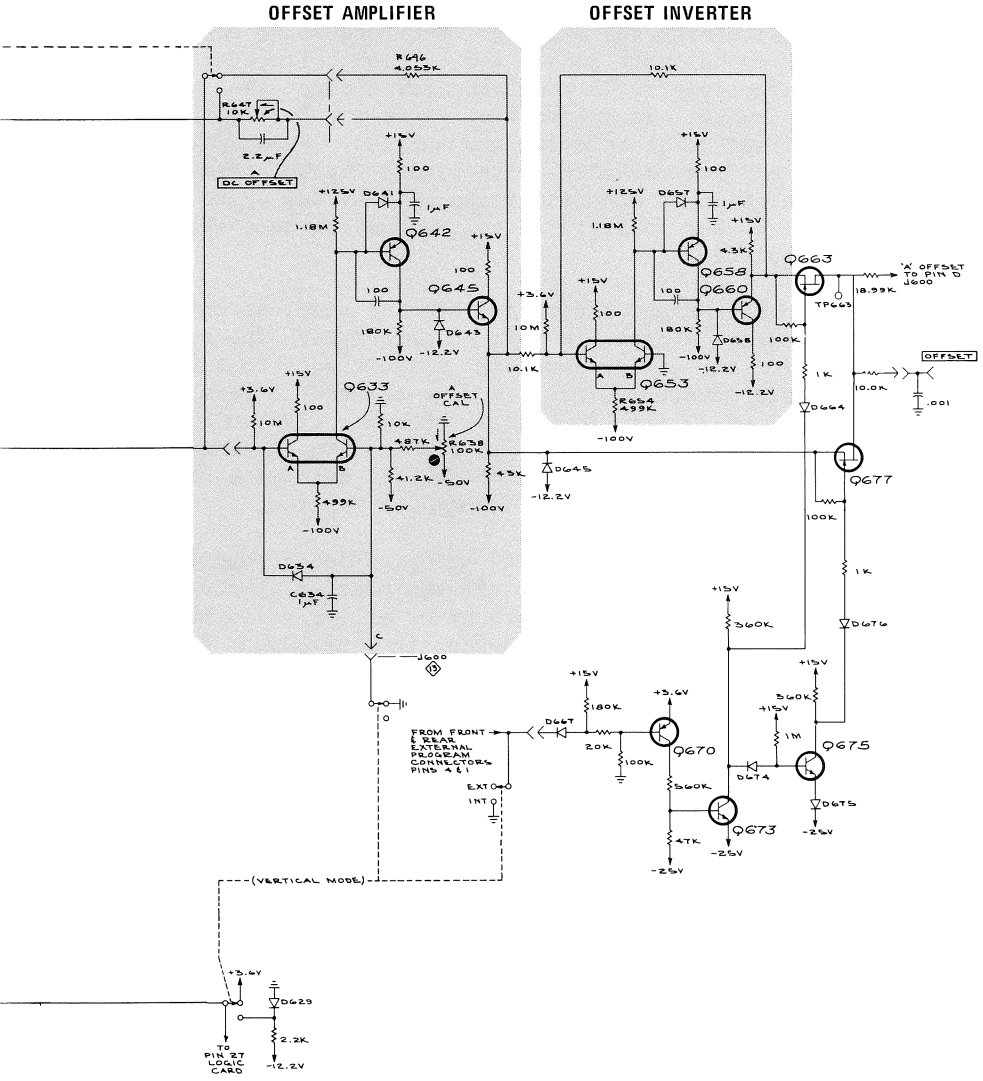


Fig. 3-8. 3S5 Ch A Programmed Offset.

3S5 CHANNEL A PROGRAMMED OFFSET CIRCUITS

In the 3S5, DC offset is used for vertically positioning the display. When operating the 3S5 from the front panel, a precision calibrated 10-turn potentiometer is available for each of the two input channels. It allows from -1 volt to +1 volt of offset to be selected and applied. When operating the 3S5 externally, with binary inputs, offset is selected in discrete steps of 5 mV and up to 995 mV of either polarity of voltage may be selected and applied.

OFFSET AMPLIFIER

Channel A and B circuits are the same, so only channel A circuits will be described. The output from the offset amplifier circuit goes to a unity-gain inverter circuit and to the source terminal of FET Q677. If FET Q677 is turned on, FET Q663 is off. The drain of each FET is common with the output so that which FET is turned on will determine whether the inverter circuit is used or bypassed.

The offset amplifier is an operational amplifier that may operate with the two bases of the dual transistor close to ground or at -10 volts below ground depending on whether the instrument is operated by an external program or from the front panel. The EXT-INT switch also changes the operational amplifier feedback path from R646, a 4.05-k resistor, to R647, the 10-k helipot. *Current* is changed through the 4.05-k resistor in the EXT position to change the offset voltage. In the INT position the *resistance* of the 10-turn 10-k variable resistor is changed to change the offset voltage; the current remains at 2 mA.

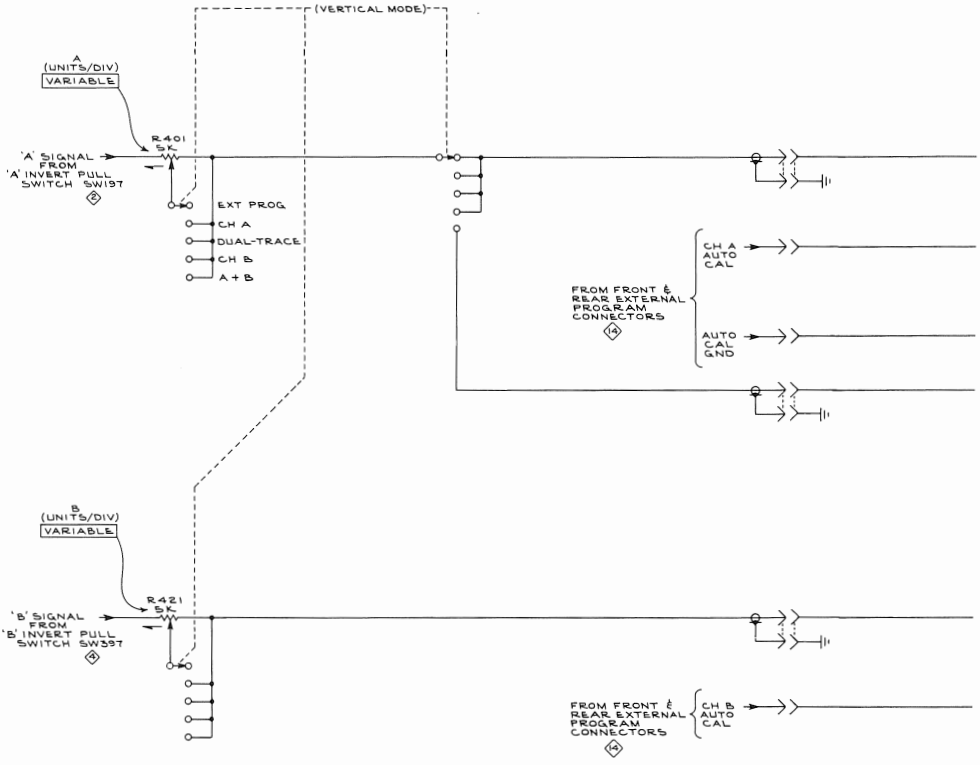
The output voltage from the offset amp only goes *up* from the voltage level of the bases of Q633 because the input current does not change direction. In the INT position the bases are at -10 volts and the output voltage may swing anywhere from -10 volts to +10 volts. In the EXT position the bases are at ground level and the output voltage from the emitter of Q645 only goes from 0 to +10 volts. However, if negative offset is programmed, the unity-gain offset inverter amplifier inverts a 0 to +10 volt swing to

a -10 volt swing and the output is coupled through FET Q663. FET Q663 is turned on when transistor Q673 turns off. Q673 is always off when Q670 is off. Grounding the appropriate input line programs a plus (+) offset voltage by turning Q670 on, Q675 off and FET Q677 on.

OFFSET CURRENT SELECTOR

Channel A and B circuits are the same so only channel A will be described. When externally programming offset voltage, the INT-EXT switch must be in the EXT position. That returns the emitters of Q602, Q610, Q616, Q620 and Q622 to +15 volts. The emitters of the other four similar transistors are always returned to +15 volts. In the EXT position, the bases of all those transistors are tied to +3.6 volts. Grounding any one of the input program leads that goes to an emitter of one of these transistors turns the transistor off. That will divert whatever current was flowing through its collector resistor to the input of the operational amplifier and cause the output voltage of the operational amplifier to change proportionally.

When operated from the front panel, with the INT-EXT switch in the INT position, five transistors are turned off by returning their emitters to ground. The bases of the other four are returned to ground instead of +3.6 volts so that unintentionally grounding their emitters externally won't turn them off. In the INT position both bases of dual transistor Q633 operate at -10 volts so there is a 40-volt drop across each collector-resistor that has been turned off. The total current should be 2 mA. Practically all of that current flows through the feedback resistor in the offset amp, and the output voltage will be proportional to the value of the variable resistor (10-turn pot). When the pot is set for precisely 5 turns, it is in the middle of its travel and its resistance is 5 kΩ. The 2 mA, which flows through that resistance, causes a 10-volt drop. The output voltage is 10 volts higher than the input base voltage, making the output zero volts with respect to ground. The offset voltage is therefore able to go above or below ground by ten volts depending on the setting of the 10-turn pot.


(VERTICAL MODE)
A (UNITS/DIV) VARIABLE
R401 5K
'A' SIGNAL FROM 'A' INVERT PULL SWITCH SW197
EXT PROG
CH A
DUAL-TRACE
CH B
A + B
FROM FRONT & REAR EXTERNAL PROGRAM CONNECTORS
CH A AUTO CAL
AUTO CAL GND
B (UNITS/DIV) VARIABLE
R421 5K
'B' SIGNAL FROM 'B' INVERT PULL SWITCH SW397
FROM FRONT & REAR EXTERNAL PROGRAM CONNECTORS
CH B AUTO CAL

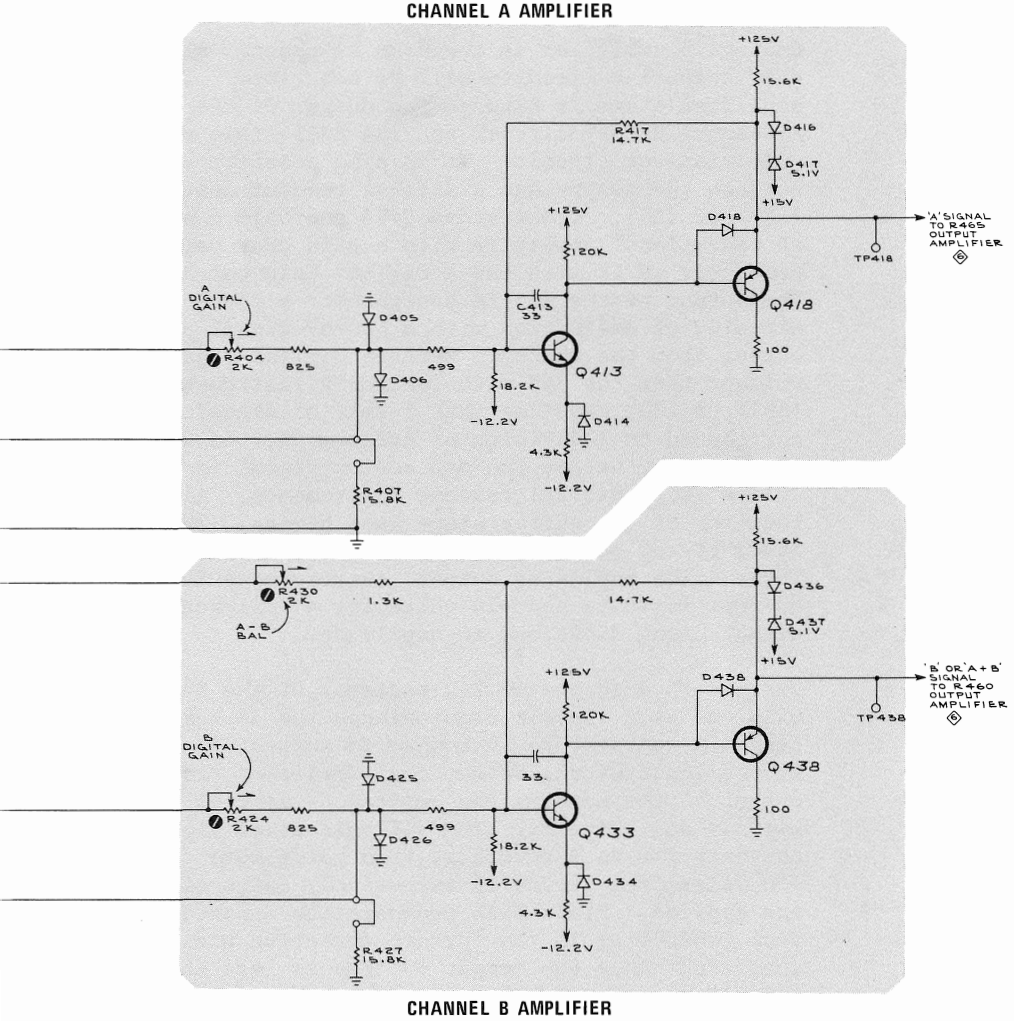


Fig. 3-9. 3S5 A and B Channel Amps.

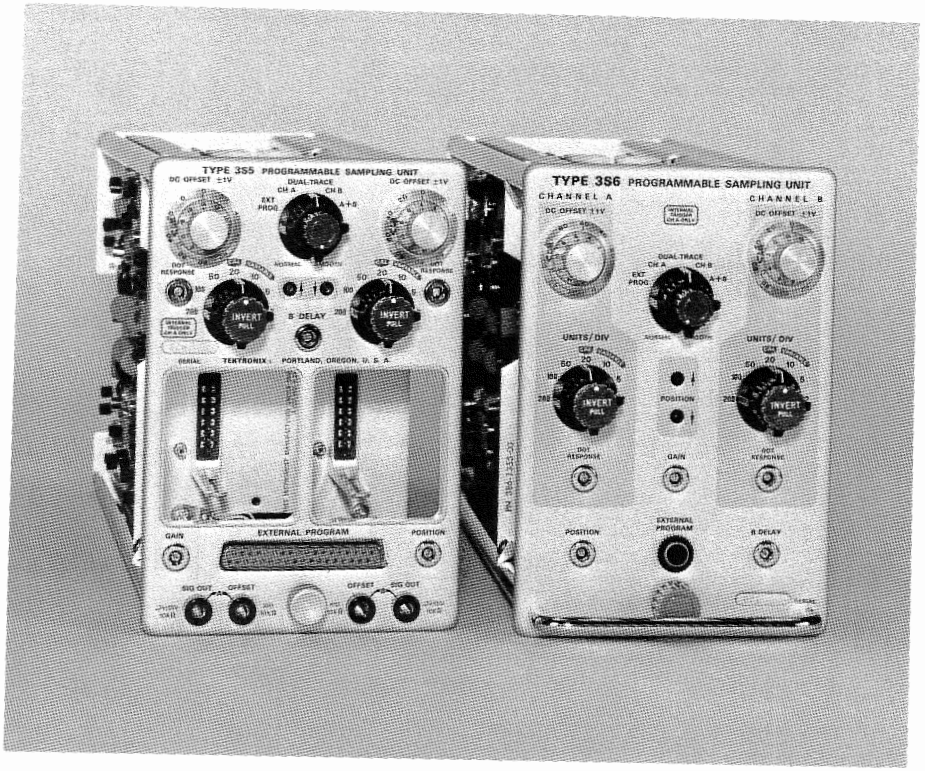
3S5 A AND B CHANNEL AMPS CIRCUITS

CHANNEL A AMPLIFIER

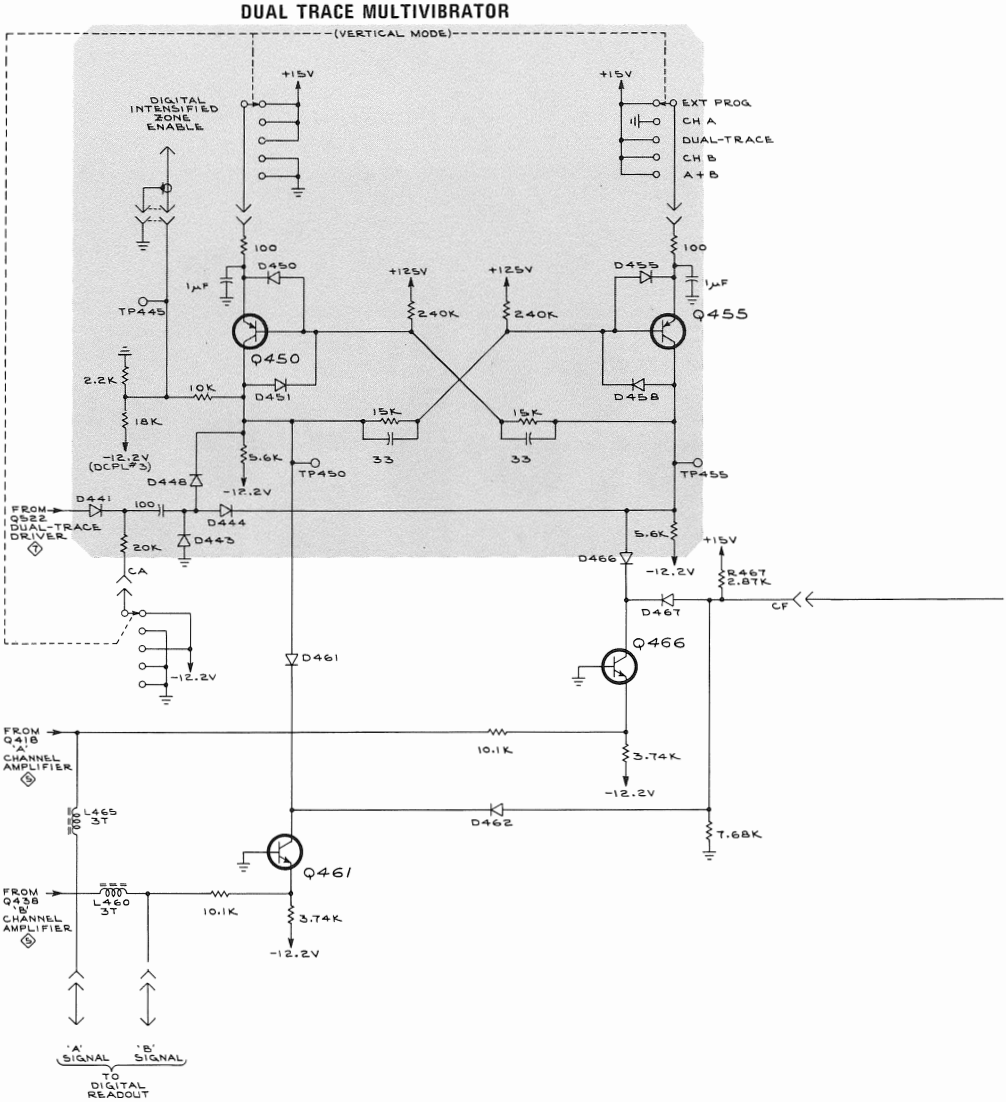
Channel B amplifier is the same as channel A so only channel A circuits will be described. This amplifier stage is between the output of the A Channel Memory circuit and the dual-trace switching multivibrator circuit. It is also a buffer stage between the memory and a digital readout instrument (6R1A or 230). Transistors Q413 and Q418 constitute an operational amplifier with a gain that can be set precisely to 2X with the A Digital Gain pot R404. The output of the 3S5 is designed to produce one division of deflection with a 500-mV signal at the output from the memory. Because digital readout of voltage from the 3S5 with Tektronix instruments (6R1A or 230) requires that 1 volt of signal correspond to 1 division of deflection, the 2X gain is necessary before the deflection signal is delivered to digital readout instruments. Also required of the buffer stage is a nominal +10 volt level at the output when there is zero volts at the input. The amplifier output, therefore, swings between +6 volts and +14 volts for a full-scale signal eight divisions in amplitude.

Current through the 18.2-k resistor at the base of Q413 causes a 10-volt drop through the 14.7-k feedback resistor so that when no current is supplied at the input of the operational amplifier from the output of the memory, the emitter of emitter follower Q418 is at +10 volts. The 5.1-volt zener diode D417 prevents the output voltage from going more than +20 volts from ground if excessively large signals are applied. Diode D416 prevents the zener diode from conducting in the forward direction under normal conditions when the output voltage is less than +15 volts.

The jumper shown at the top of resistor R407 is removed when it is desirable to automatically adjust the gain of the amplifier (with special equipment) to reduce measurement errors of voltage to a minimum for any sensitivity.


TYPE 355 PROGRAMMABLE SAMPLING UNIT
TYPE 3S6 PROGRAMMABLE SAMPLING UNIT
CHANNEL A
CHANNEL B
DC OFFSET ±1V
DUAL-TRACE
EXT PROG
INVERT PULL
B DELAY
TEKTRONIX
PORTLAND, OREGON, U. S. A.
UNITS/DIV
POSITION
GAIN
EXTERNAL PROGRAM
SIG OUT
OFFSET

DUAL TRACE MULTIVIBRATOR



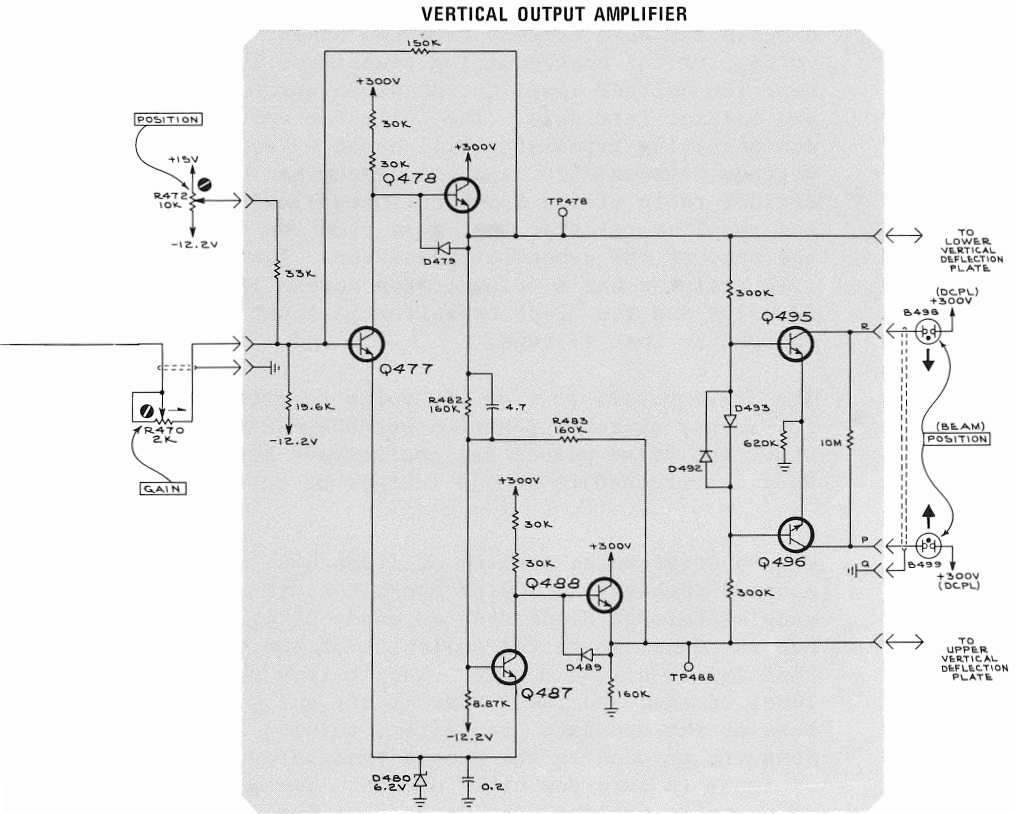


Fig. 3-10. 3S5 Output Amplifier.

3S5 OUTPUT AMPLIFIER CIRCUITS

DUAL-TRACE MULTIVIBRATOR

When dual-trace operation has been selected, the bistable multivibrator transistors alternately turn on and off each time a drive pulse arrives at the input to diode D441. When transistor Q450 is on, transistor Q455 is off, and vice-versa. In the dual-trace mode the emitters of both transistors are returned to +15 volts. Whichever transistor conducts diverts the base current from the other. The base voltage of the nonconducting transistor is clamped near its emitter level by the diode across its base and emitter terminals. The collector voltage of the nonconducting transistor will be at -5 volts, a voltage between -12.2 and +15 determined by the divider ratio of the 5.6-k collector-load resistor and the 15-k resistor that goes from the collector to the base of the opposite transistor. That means the 15-k resistor has a voltage drop across it of about 20 volts and the 33-pF capacitor in shunt with it is charged to that voltage.

The drive pulses go from -50 volts to ground and back. So, in any switched position but DUAL-TRACE or EXT PROG, the drive pulses are ineffective because diode D441 is returned to ground instead of to -12.2 volts.

When a drive pulse arrives at diode D441 and is coupled through the 100-pF capacitor, it also is coupled through diode D448 or diode D444, whichever one is connected to the collector of the transistor that is off at the moment. That raises the collector level of the transistor that is off and with it the base of the opposite transistor, turning it off also. However, as soon as the second transistor turns off, it tends to turn the other one on. Then, when the drive pulse expires, the transistor that was not conducting turns on and the one that was conducting turns off. The reason for the reversal is that one

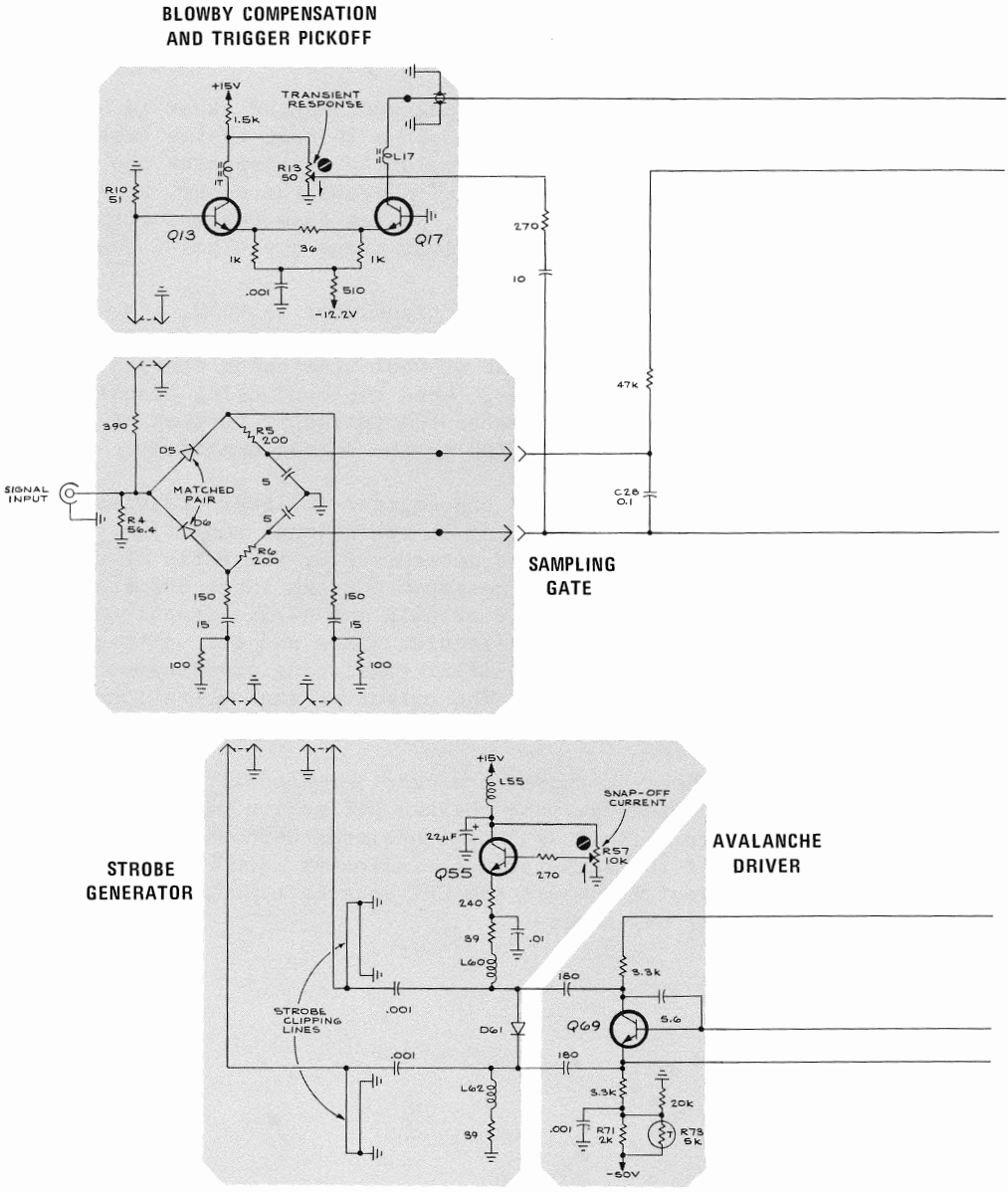
33-pF capacitor is charged and the other is not. The one which has about a 20-volt charge remaining in it has a charge polarity that opposes the applied forward base voltage, whereas the other, being almost entirely discharged, passes base current first. The one that conducts first keeps the other turned off.

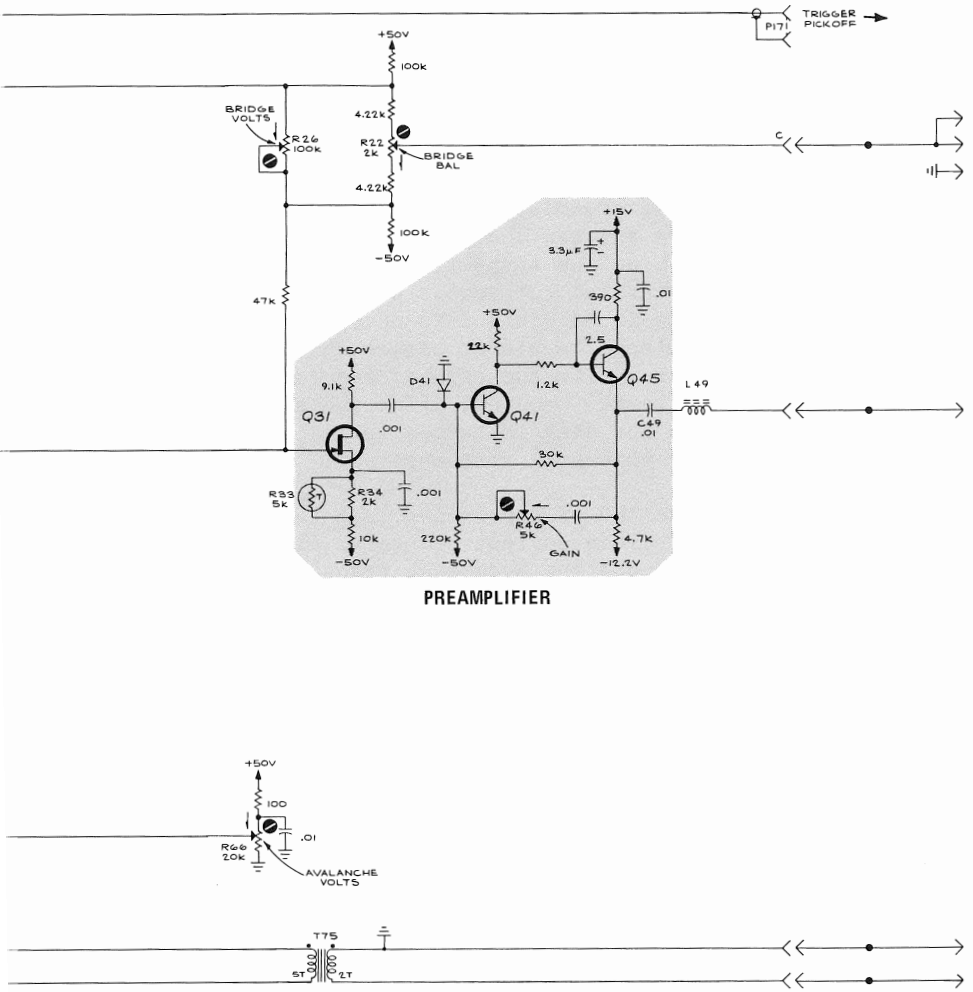
When the conducting transistor is Q450, its collector voltage goes up high enough to divert the collector current of Q461 from being coupled to the output amplifier. When the conducting transistor is Q455, it diverts the collector current of Q466 from being applied to the output amplifier.

VERTICAL OUTPUT AMPLIFIER

Transistor Q477 and emitter-follower transistor Q478 are a part of an operational amplifier, the gain of which is determined by the ratio of the 150-k feedback resistor and the input resistance, comprised partly of GAIN pot R470. Transistor Q478 drives a CRT deflection plate and the unity-gain operational amplifier consisting of transistors Q487 and Q488. The output of that operational amplifier drives the other CRT deflection plate.

Whenever there is a considerable difference in voltage between the two deflection plates, either transistor Q495 or transistor Q496 will turn on one of the beam-position-indicator neon bulbs to indicate where the CRT beam is aimed, if extinguished or off-screen.


BLOWBY COMPENSATION
AND TRIGGER PICKOFF
+15V
1.5k
TRANSIENT RESPONSE
R13 50
CL17
R10 51
Q13
Q17
1k
36
1k
.001
510
-12.2V
270
10
47k
C28 0.1
390
D5
R5 200
SIGNAL INPUT
MATCHED PAIR
D6
R4 56.4
R6 200
5
5
150
15
100
150
15
100
SAMPLING GATE
STROBE GENERATOR
+15V
L55
SNAP-OFF CURRENT
22μF
Q55
R57 10K
270
240
39
.01
L60
STROBE CLIPPING LINES
.001
D61
.001
L62
39
180
3.3k
Q69
5.6
180
3.3k
20k
.001
R71 2k
R73 5k
-60V
AVALANCHE DRIVER



PREAMPLIFIER

Fig. 3-11. S-1 Sampling Head.

S-1 SAMPLING HEAD CIRCUITS

AVALANCHE DRIVER and STROBE GENERATOR

Transistor Q69 has very fast avalanche breakdown characteristics. It is normally not conducting but is adjusted to have *nearly* enough collector-to-emitter voltage to avalanche without a turn-on pulse being applied. When resting, its emitter will be about 45 volts below ground and its collector somewhere between zero and +50 volts. When the base of the avalanche transistor receives a sampling-command pulse, the transistor suddenly becomes a very low impedance and the charge in the two 180-pF capacitors reverse bias the snap-off diode D61 and rapidly sweep out its current carriers. With the carriers gone, the diode is suddenly like an open circuit and a very steep voltage wavefront passes through the two .001-μF capacitors. The two strobe clipping lines look like a short circuit, however, after the two-way propagation time, so the step is turned into a pair of short duration push-pull strobe pulses.

After the 180-pF capacitors lose their charge, snap-off diode current starts to flow in the forward direction and the avalanche transistor current diminishes to zero. The 180-pF capacitors then recharge and make the avalanche driver circuit ready for the next sampling-command pulse.

Avalanche voltage is somewhat dependent on temperature so the 5-k thermal element which shunts the 2-k divider resistor in the emitter circuit of Q69 changes the avalanche voltage slightly as temperature changes to assure stable operation over a wide range of temperatures.

Transistor Q55 is an emitter follower that determines the amount of forward current which flows through the snap-off diode. The Snap-Off Current potentiometer, R57, is normally adjusted for the best compromise between noise and risetime within specified limits. If two S-1 sampling heads are used for dual-trace displays, precise equality of risetime may be important.

SAMPLING GATE

Sampling gate diodes D5 and D6 are back biased by the voltage drop across the Bridge Volts potentiometer R26, which is normally adjusted for maximum voltage. Push-pull strobe pulses from the strobe generator circuit are of the right polarity to overcome the back bias and turn both diodes on to admit a sample of the signal. Whenever the signal voltage at the input is a different value from the previous sample, there will be a difference in voltage between the input and the output of the bridge. That will cause one input diode to conduct harder and the other to conduct less, causing either a positive or negative output step to be applied to the input of the sampling preamp. The step will then be amplified and admitted to the memory capacitor and fed back to the center arm of the Bridge Bal potentiometer. That moves the level of the sampling preamp input toward matching the level of the signal when last sampled.

With two-diode sampling gates there is a permanent but inconsequential voltage difference between the level of the preamp input and the voltage fed back from the memory. That voltage is one half of the corner-to-corner bridge voltage.

The 56.4-ohm resistor at the input to the sampling gate, in shunt with the 390-ohm and 51-ohm resistor used for signal pickoff, provide the needed 50-ohm input termination.

BLOWBY COMPENSATION

Blowby is a term that describes a transient response aberration caused by high-frequency signal components being coupled through the capacitance of the sampling gate diodes even when they are back biased. High-frequency signal components are not blocked by the back bias but "blow" right by -- through the capacitance. Whenever the input voltage of the preamplifier is altered as a result of a charge that couples through the diode capacitance, the sampling-loop amplifiers try to respond. When the memory gate passes an amplified signal which is a mixture of the

sampled voltage and the voltage resulting from blowby, the displayed signal will probably be distorted. To reduce the effect to a minimum an AC-coupled wideband inverting amplifier with the right gain and time constants can be placed in shunt with the sampling gate to neutralize the effect. That way, essentially all the current coupled through the diode capacitance passes through the output of the inverting amplifier and does not produce a voltage change at the input to the sampling preamp.

Transistor Q13 is the inverting amplifier and provides current gain. Transient response adjustment R13 determines the amount of high-frequency neutralizing current that will be coupled to the output of the sampling gate. The 10-pF capacitor and 270-ohm resistor in series with the output lead are the principle time constant determining elements.

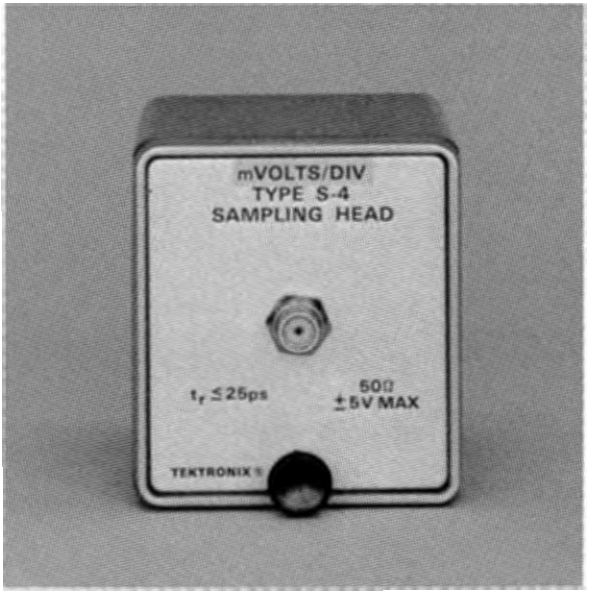
TRIGGER PICKOFF

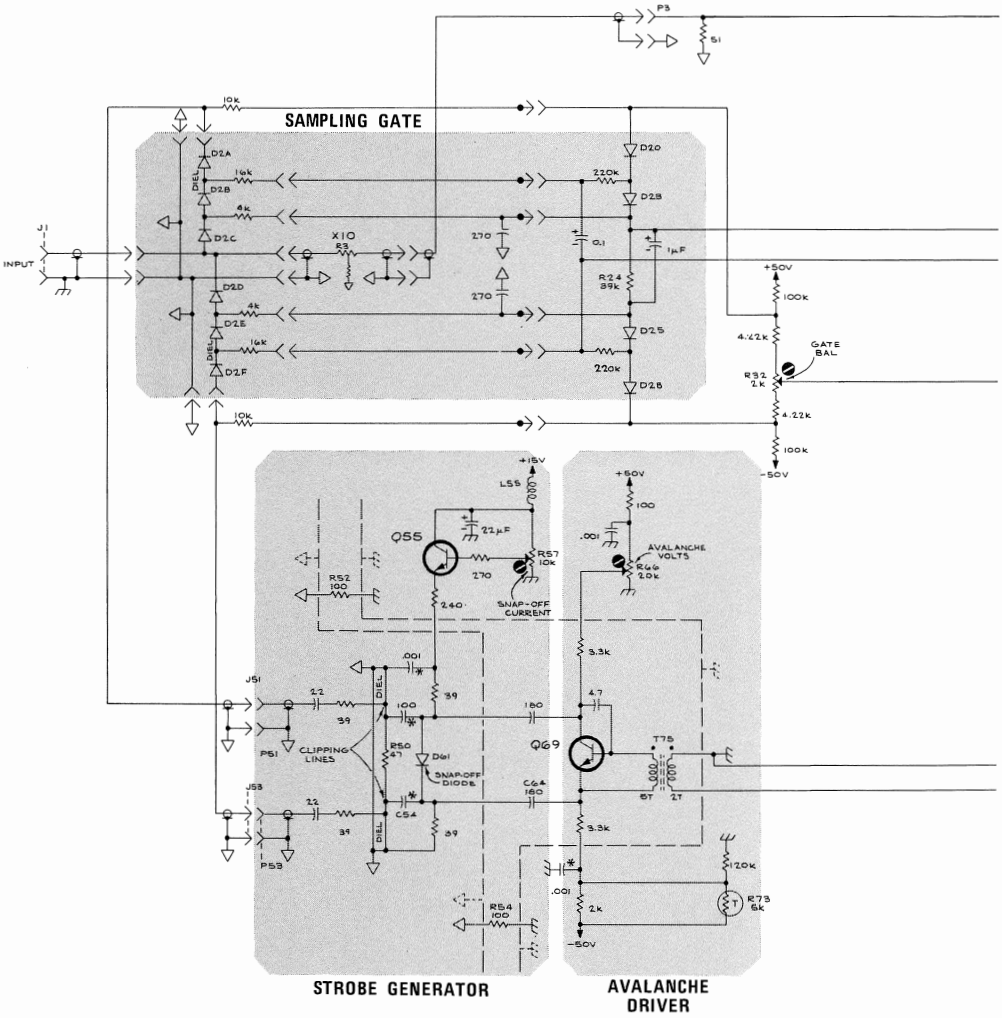
The emitter of grounded base transistor Q17 is driven by the emitter of Q13 through the 36-ohm resistor that separates them. The signal at the collector of Q17 may be used for a triggering signal.

PREAMPLIFIER

FET Q31 is operated with essentially constant current to assure constant gain. The thermal element in the FET source circuit compensates for most changes in current that might result from a change in temperature. The source is bypassed with a .001-μF capacitor to provide maximum gain for the short intervals when the sampling amplifiers must operate. Transistors Q41 and Q45 are a self-biasing DC-coupled fedback pair with low output impedance. Gain adjustment for the stage is set with R46. This control and the loop-gain adjustment in the plug-in unit that accommodates the S-series sampling heads both control the sampling-loop gain. To assure compatibility of adjustment range when interchanging sampling heads, a special Normalizer Head (067-0572-00) should be used.


mVOLTS/DIV
TYPE S-1
SAMPLING HEAD
$t_r \leq 350ps$
TEKTRONIX
50Ω
±5V MAX


mVOLTS/DIV
TYPE S-4
SAMPLING HEAD
$t_r \leq 25ps$
50Ω
±5V MAX
TEKTRONIX


SAMPLING GATE
INPUT
J1
10k
D2A
D2B
D2C
D2D
D2E
D2F
DIEL
16k
4k
X10
R3
270
270
D2C
D2B
D2E
D2F
220k
220k
0.1
1µF
R24
39k
+50V
100k
4.42k
GATE BAL
R32
2k
4.22k
100k
-50V
10k
+15V
L55
Q55
22µF
R57
10k
270
240
SNAP-OFF CURRENT
R52
100
.001
J51
22
39
DIEL
100
39
180
4.7
3.3k
P51
CLIPPING LINES
R50
47
D61
SNAP-OFF DIODE
Q69
T75
.001
.001
5T
2T
J53
22
39
C54
C64
160
39
3.3k
P53
120k
.001
2k
R73
6k
R54
100
-50V
+50V
100
.001
AVALANCHE VOLTS
R46
2.0k
STROBE GENERATOR
AVALANCHE DRIVER

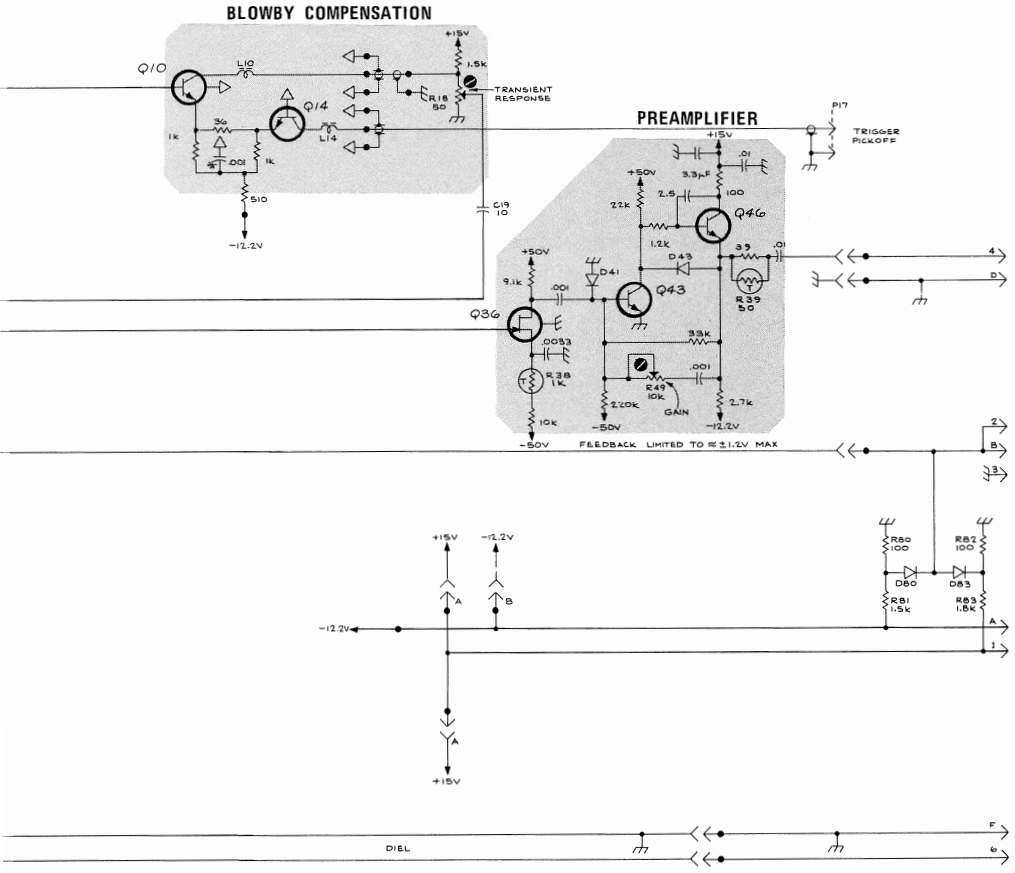


Fig. 3-12. S-4 Sampling Head.

S-4 SAMPLING HEAD CIRCUITS*

SAMPLING GATE

The sampling gate circuit used in the S-4 sampling head is uniquely different in design, construction and concept. Six sampling gate diodes are used, instead of two or four as in other sampling gates. They are constructed of chips mounted in series in a segment of the center conductor portion of a three-plane, 50-ohm strip-line transmission line. In the diagram the diodes are D2A, D2B, D2C, D2D, D2E and D2F. Most of the time they are all back biased and they are only turned on when it is desirable to admit a sample of the input signal voltage. The input signal is applied at all times to the point in the middle of the string where diode D2C joins diode D2D. The signal is introduced to the midpoint of the diode string via a conductor which is also part of the three-plane, 50-ohm strip-line environment but is brought in at right angles to the diode string. Permanently connected near that point also, is a miniature 50-ohm termination that also provides, at a 10-to-1 reduction in amplitude, signal pickoff for blowby compensation and triggering.

The risetime of the S-4 does not depend on the width of the strobe pulses as do other earlier sampling gates. Instead, the risetime is dependent on how fast the sampling diodes may be turned off, or on what the signal propagation time between diodes may be, or a little bit of both. The principle of sampling with the S-4 is to capture the signal energy in a segment of a transmission line and amplify it. With this principle, risetime would be dependent only on the length of the segment between diodes if the diode-switches could be opened instantly and simultaneously. In that case, the risetime would be equal to the propagation time through the segment. If the switches were not opened simultaneously, but opened at instants that were separated by an amount of time equal to the propagation time, the risetime would be equal to twice the propagation time through the segment. Such a case exists in the S-4. Diodes are used for switches and are turned off by the trailing edge of a strobe pulse that is launched in the opposite direction to the input signal energy.

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*See S-1 for description of Avalanche Driver, Strobe Generator, Blowby Compensation and Preamp Circuits.

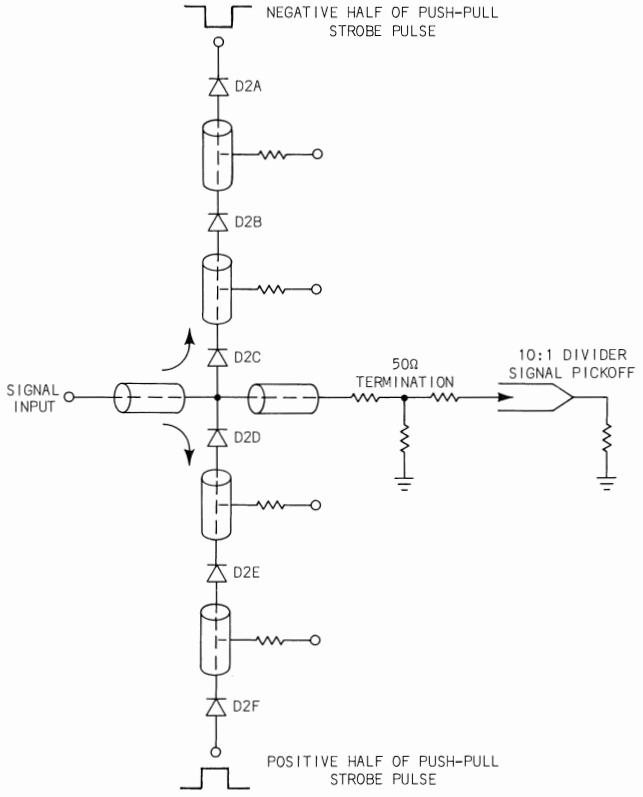


Fig. 3-13. Sampling-gate input.

To make the sampling gate a balanced type of gate, signal energy is allowed to flow into two divergent paths instead of just one path and a push-pull strobe pulse makes the diodes conduct. Fig. 3-13 illustrates the input arrangement. Coaxial transmission line segments are shown between diodes.

Diodes D2A and D2F are turned on simultaneously when the leading edge of the push-pull strobe pulses arrive. Slightly later, diodes D2B and D2E are turned on by the same pulse edges and finally diodes D2C and D2D are also turned on. At that instant, signal energy flows in two new directions -- through both diode D2C and diode D2D toward opposite ends of the

string of diodes. When the strobe pulse ends, diode D2A and D2F turn off simultaneously, then diode D2B and D2E turn off and finally diode D2C and D2D turn off. The signal voltage captured between the outer two pairs of diodes is applied to the input of the sampling preamplifier. Then they are amplified for a few hundred nanoseconds by the following stages and held in the memory capacitor until the next sample is taken.

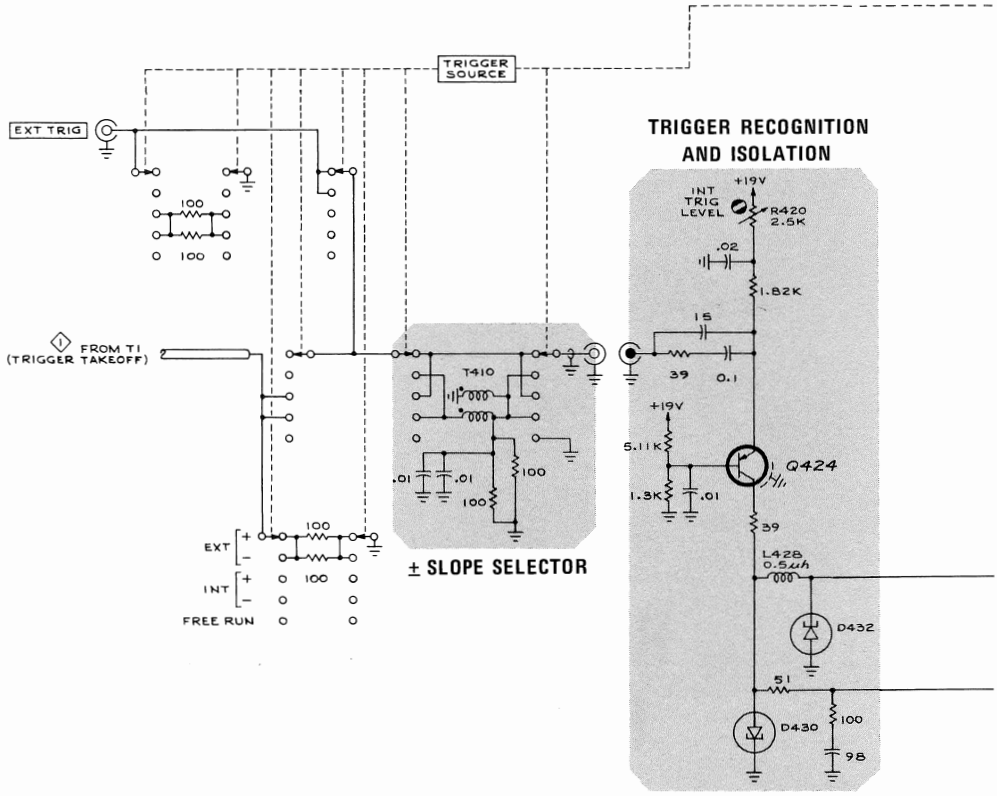
The signal charge trapped between diodes D2A and D2B is practically the same as that trapped between diodes D2E and D2F. Both charges are transferred through the two 16-k resistors into the preamplifier input capacitance. The transfer takes place right after each strobe pulse ends. The two charges are transferred in a short time (about 10 nanoseconds) because the effective capacitance of each segment between diodes is very small. The following sampling amplifier stages have several hundred nanoseconds to respond to each new sample before the memory gate circuit interrupts current flow through the memory capacitor. So, even though the step signal at the input to the sampling preamplifier is not as abrupt as with other sampling gates, there is adequate time to amplify each sample.

The back-bias circuit for the sampling-gate diodes consists of diodes D20, D23, D25, D28, all of which are passing the same forward current through the 39-k resistor in the middle of the string. Most of the back-bias voltage is developed across the 39-k resistor and is applied across sampling-gate diodes D2C and D2D through the two 4-k isolation resistors. Additional voltage drop, about 0.5 volts per diode, is provided by diodes D20, D23, D25 and D28. Those four diodes back bias each of the four sampling-gate diodes. For example, the forward voltage drop across diode D20 is back bias for diode D2A.

Blowby compensation for sampling-gate diode capacitance is fed back to the diode string through the two 4-k resistors. If it were not for the need to compensate for blowby, the sampling gate could be made with four diodes instead of six.

4

RAMP TRIGGERING AND RAMP DELAY CIRCUITS


TRIGGER SOURCE
EXT TRIG
100
100
FROM T1
(TRIGGER TAKEOFF)
T410
.01
.01
100
100
EXT
INT
FREE RUN
100
100
± SLOPE SELECTOR
TRIGGER RECOGNITION AND ISOLATION
+19V
INT TRIG LEVEL
R420 2.5K
.02
1.82K
15
39
0.1
+19V
5.11K
1.3K
.01
Q424
39
L428 0.5μh
D432
51
D430
100
98

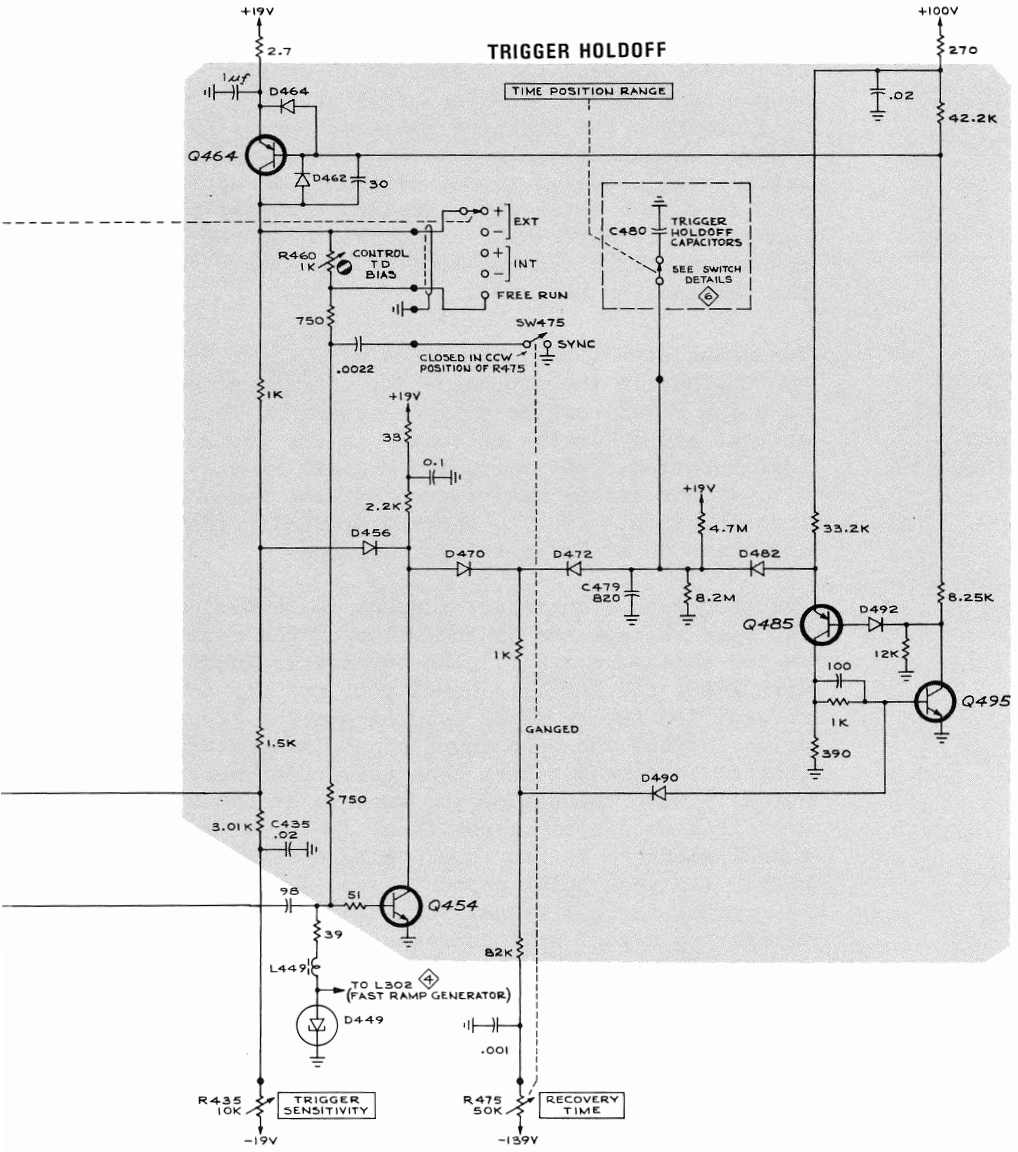


Fig. 4-1. 1S1 Trigger.

1S1 TRIGGER CIRCUITS

± SLOPE SELECTOR

When triggering on the plus slope of an input triggering signal, the signal is AC-coupled directly to the emitter of isolation transistor Q424. When triggering on the negative slope of the triggering signal, the polarity is reversed by transformer T410 before being coupled to the emitter. An approximate 50-Ω impedance match is maintained for most frequency components by matching the inductance of the transformer with the two 0.01-μF capacitors that shunt the termination resistors.

TRIGGER RECOGNITION and ISOLATION

The transistor Q424 is operated with about +5 volts on the base in the grounded-base configuration. An up-going signal on the emitter causes an increase in emitter and collector current. In the grounded-base configuration, fast switching signals in the collector circuit are fairly well prevented from feeding back into the input circuit, thereby providing the needed isolation to minimize trigger kickout.

The zero-signal collector current is determined by the base voltage and by the value of the resistors in the emitter circuit. The current is adjustable with R420, the Int Trig Level pot, and set so the recognition tunnel diode D430 is passing its peak point current when the front panel TRIGGER SENSITIVITY control is somewhat less than fully clockwise -- normally when the dot on the knob is at about the 2 o'clock or 3 o'clock position. When the recognition tunnel diode is in its lower voltage state and passing nearly its peak point current, even a small increase in current through transistor Q424 caused by the input triggering signal will increase current through the tunnel diode enough to make it switch to its higher voltage state. If control tunnel diode D449 had been armed at that instant, it will be switched to its higher voltage state by energy which passes through the 51-ohm resistor, 98-pF capacitor, 39-ohm resistor and the small inductor L449 that couples the first tunnel diode to the second. When the second tunnel diode switches to its higher voltage state, its output causes a fast ramp to start. That output is the principle output in the whole trigger and holdoff circuit.

At the end of a holdoff interval Q464, in the trigger holdoff circuit, is turned on and supplies arming current to both tunnel diodes. In all modes, except the SYNC mode, arming current is supplied to both tunnel diodes almost simultaneously. In the SYNC mode, used for ultrahigh-frequency signals, arming current for the control tunnel diode D449 is diverted momentarily while a capacitor charges. The .0022-μF capacitor at the junction of the two 750-ohm resistors in the trigger holdoff circuit is connected to ground only in the SYNC mode. When it is fully charged, the control tunnel diode should pass nearly its peak point current. The Control TD Bias adjustment, R460, allows us to set the bias current at a stable value between the peak point current threshold and a low current threshold. When the current is set too low, the recognition tunnel diode cannot cause the control tunnel diode to switch to its higher voltage state. If set too close to the peak point current, a change in temperature may make the peak point current to be reduced and cause erratic triggering or a free-run condition.

In the SYNC mode the recognition tunnel diode may switch up and down quite a few times before causing the control tunnel diode to switch up even once. In fact, in this mode the recognition tunnel diode can be made to continually oscillate even in the absence of a triggering signal if the TRIGGER SENSITIVITY control is set far enough clockwise. The circuit oscillates because of the negative resistance characteristics of the tunnel diode. The frequency of oscillation is roughly 30 MHz, depending on the L/R ratio of the inductor L428 and the combined series resistances of the recognition tunnel diode D430 and back diode D432. The oscillation frequency will be "pulled" by the input triggering signal so that with the proper setting of the TRIGGER SENSITIVITY control the frequency of oscillation can be set to be a subharmonic of the input triggering signal. A countdown frequency divider action takes place. After a few cycles, the control tunnel diode becomes armed and responds to the first up-going portion of the subsequent cycle, starting a fast ramp in sync with the triggering signal.

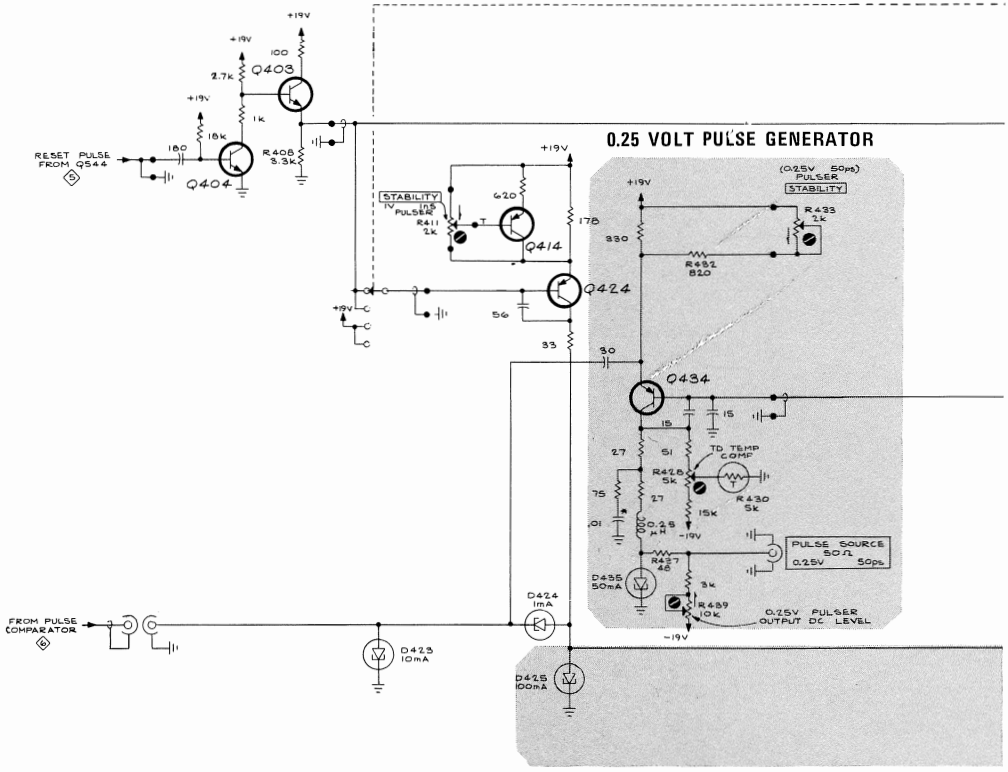
TRIGGER HOLDOFF

Trigger holdoff begins the instant the control tunnel diode D449 switches to its higher voltage state and starts a fast ramp. The increase in voltage drop across the control tunnel diode turns on transistor Q454. Prior to that, only about +100 mV appeared across the base-emitter junction, not enough to turn the transistor on. When the transistor turns on, it diverts current that was flowing through the recognition tunnel diode D430 by lowering the voltage at the junction of the 1-k and 1.5-k resistors. That holds off further tunnel diode trigger signals for awhile. For the tunnel diode arming current transistor Q464 to be turned on, multivibrator transistor Q495 also has to be turned on. The other multivibrator transistor Q485 is also on when Q495 is on. Therefore, before the triggering signal is recognized, all three transistors must be on. And they all remain on for a while after the triggering signal is recognized.

At the beginning of a holdoff interval, when Q454 turns on, current that had been flowing through R475, the RECOVERY TIME control, no longer passes through diode D470 and the 2.2-k resistor connected to its anode but flows instead through diode D472. That discharges the holdoff capacitor C479 and any other holdoff capacitor that may be switched in parallel with it, depending on the TIME POSITION RANGE selected. As the holdoff capacitor discharges downward and the voltage level at the junction of the 1-k resistor and the 82-k resistor, in series with the RECOVERY TIME control, starts to go below ground, diode D490 starts to conduct. That tends to turn off transistor Q495 which tends to turn off Q485. The action is regenerative and both transistors suddenly switch off. That turns off transistor Q464 which interrupts the control tunnel diode current. The tunnel diode thereupon switches back to its low voltage state and allows the fast ramp to recover.

The run-down time of the holdoff capacitor(s) determines how long a fast ramp may run before being signaled to reset. The fast ramp reset interval (last part of the holdoff interval) begins when the control tunnel diode switches to its low voltage state. That turns off transistor Q454 which diverts current from D472 and directs it through diode D470. The holdoff capacitor then starts to run back up. Most of its current passes through diode D482 and the 33.2-k resistor that goes to the +100 volt supply. The run-up slope is a function of the size of the holdoff capacitor(s). Run-up, and the holdoff interval, ends when the emitter voltage of transistor Q485 starts to go higher than its base voltage. At that instant transistor Q485 starts to turn on, which turns on Q495, which helps turn on Q485. Both transistors suddenly turn on hard which turns on Q464 and re-arms the tunnel diodes in the trigger recognition circuit. The base voltage of Q485 is set by the divider action of the 12-k and 8.25-k resistors in the base circuit. The top side of the 8.25-k resistor is clamped at +19 volts by diode D464.

The next triggering signal may then be recognized and a new fast ramp initiated. Or, in the FREE RUN mode, a fast ramp may be initiated immediately. In that mode, R460 is shorted by the FREE RUN switch and more than the peak point current of the control tunnel diode is delivered to it, causing it to immediately switch to its higher voltage state. In the FREE RUN mode fast ramps and strobe signals are generated at a maximum rate for each time position range. That rate is somewhat variable depending on the setting of the RECOVERY TIME control. Varying the RECOVERY TIME varies the slope of the rundown portion of the holdoff capacitor by controlling the amount of current flowing through the holdoff capacitor(s).


0.25 VOLT PULSE GENERATOR
RESET PULSE FROM Q544
Q403
Q404
Q414
Q424
Q434
R408 3.3K
R411 2K
R428 5K
R430 5K
R433 2K
R437 4Ω
R439 10K
R492 820
STABILITY
PULSER
(0.25V 50ps) PULSER
PULSE SOURCE 50Ω 0.25V 50ps
TD TEMP COMP
0.25V PULSER OUTPUT DC LEVEL
FROM PULSE COMPARATOR
D424 1mA
D423 10mA
D425 100mA
D435 50mA
+19V
-19V

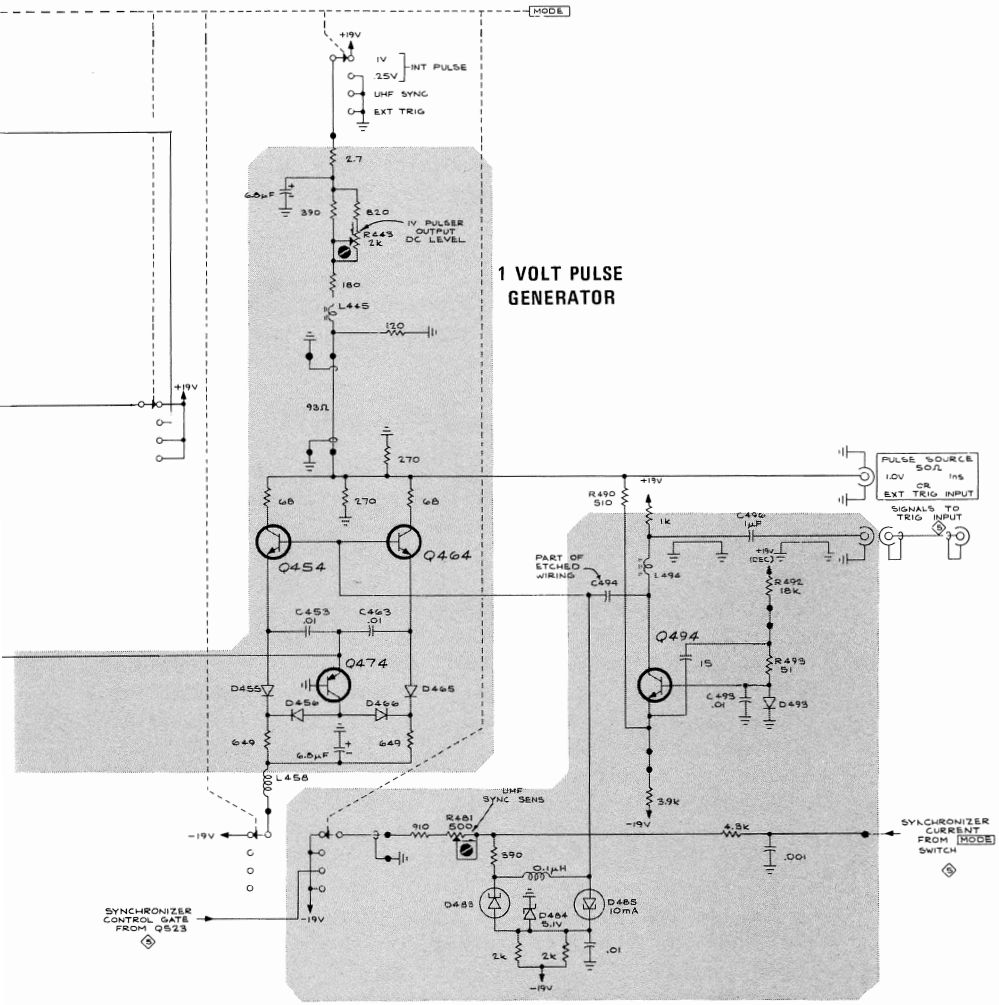


Fig. 4-2. 1S2 Pulse Generators.

1S2 PULSE GENERATORS (AND TRIGGER INPUT) CIRCUITS

TRIGGER ISOLATION

When the 1S2 is used as a general purpose sampler, neither of the two TDR pulse generator circuits are operative. The connector used as an output when the 1-volt pulse is being generated is used as an input for the triggering signal. No input triggering circuits are needed when generating output pulses because the pulses are automatically generated in sync with the free-running fast ramp and holdoff circuits.

An input triggering signal is DC-coupled to the emitter of trigger isolation transistor Q494 by way of the 510-ohm resistor connected to its emitter. The collector of that transistor couples most of the output signal through the 1-μF capacitor over to the slope selector in the trigger circuits.

UHF SYNC OSCILLATOR

A portion of the signal at the collector is coupled over to tunnel diode D485 through capacitance C494 and, when the UHF SYNC mode is selected, influences the frequency of the UHF sync oscillator. The UHF sync oscillator does not oscillate when the EXT TRIG mode is selected, or when generating either of the TDR pulses. The oscillator is comprised of tunnel diode D485, back diode D483 and the 0.1-μH inductor between them. Its frequency is mostly dependent on the L/R ratio of the inductor and the equivalent series resistance of the back diode and the tunnel diode. But the frequency may be influenced by (1) the frequency of the signal coupled through capacitance C494, (2) the bias current supplied to the tunnel diode through UHF Sync Sens control R481 and (3) the amount of bias current diverted through the 4.3-k resistor. The bias current diverted through the resistor depends on the position of the front panel TRIGGER SENS or UHF SYNC knob. When synchronizing on a UHF signal the oscillator is adjusted to oscillate at a frequency which is a subharmonic of the UHF input signal and it couples its energy back through capacitance C494 and the 1-μF capacitor to the slope selector in the triggering circuits.

The tunnel diode and back diode are operated at -5.1 volts, set by zener diode D484. In either of the two INT pulse modes, when the TDR pulses are generated, the tunnel diode does not receive any bias current. In fact, reverse current flows through the tunnel diode because R481 is returned to a negative voltage instead of being gated to a positive level by holdoff transistor Q523. The -5.1 volt zener diode fixes the base level of transistors Q454 and Q464 in the Pulse Generator circuit.

1-VOLT PULSE GENERATOR

The 1-volt step signal is generated by suddenly turning off the collector current flowing through transistors Q454 and Q464. When the current flows, the voltage at the pulse output terminal should be zero volts and is adjusted to that value with R443, the 1-V Pulser Output DC Level potentiometer. When that control is adjusted correctly, all the collector current passing through Q454 and Q464 also passes through the 93-ohm cable and the 180-ohm resistor at the top end of the cable.

Before a pulse is generated, the 100-mA tunnel diode D425 that is connected to the emitter of Q474 is in its lower voltage state and Q474 is cut off. When the tunnel diode switches to its higher voltage state, it turns on Q474 and diverts emitter current from both Q454 and Q464. When those transistors turn off, the voltage at their collectors rises and a step voltage approximately 1 volt in amplitude is generated. The 93-ohm cable in parallel with the other resistors at that point makes the source impedance look like 50 ohms. The current which passes through the two transistors is determined by the -5.1 volts on their bases and the value of the resistors in the emitter circuits. The amount of current determines the size of the output step signal.

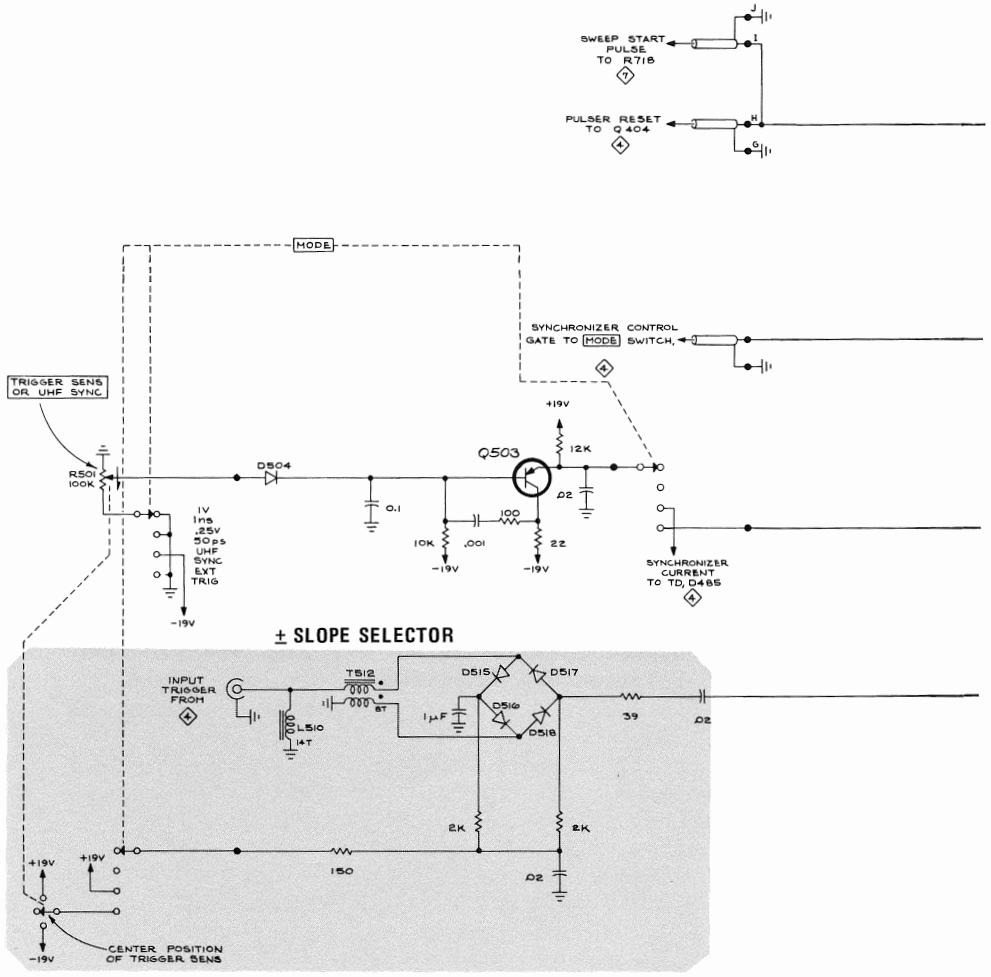
0.25-VOLT PULSE GENERATOR

The output from the 0.25-volt step generator is directly from 50-mA tunnel diode D435 through a 48-ohm resistor. The tunnel diode has a dynamic resistance of about 2 ohms so the pulse source impedance is close to 50 ohms. To make the output voltage precisely zero volts when the tunnel diode is in its lower voltage state, some current is passed through the 48-ohm resistor through R439, the 0.25-volt Pulser Output DC Level potentiometer. Bias current for the tunnel diode is determined by the base voltage of transistor Q434 and the value of the resistance in its emitter circuit. The base voltage depends on the ratio of the 2.7-k and 1-k resistors in the collector circuit of Q404, which is saturated except when the 50-mA tunnel diode is being reset. The STABILITY potentiometer R433 is used to set the bias current at a stable value just below the peak point current of the tunnel diode. Because the peak point current of the tunnel diode may change somewhat with temperature, TD Temp Comp potentiometer R428 may be set so the thermal element R430 can change the current as needed to track with temperature changes.

The 0.25-volt pulse generator tunnel diode is switched to its higher voltage state when the input trigger tunnel diode D423 is switched to its higher voltage state. The positive pulse edge coupled to the emitter of Q434 increases current through Q434 momentarily. The network of components in the collector circuit of Q434 helps keep the output step as free from aberrations as possible while delivering the fastest possible transition.

The tunnel diode D435 is reset to its lower voltage state by a negative step at the input to transistor Q404 from the holdoff circuit. Q404 turns off, raises the base level of emitter follower Q403 to +19 volts and momentarily reduces the collector current of Q434 below the valley point current of tunnel diode D435. When the reset pulse ends, the tunnel diode current increases to an amount just below its peak point value until again triggered.

The 100-mA tunnel diode D425 and the 10-mA trigger-regenerator tunnel diode D424 are reset and armed in the same way. The 1-mA tunnel diode D424 is used as a low-voltage tunnel rectifier to isolate the input from the 100-mA tunnel diode. When the 10-mA tunnel diode is switched to its higher voltage state, it biases the tunnel rectifier in its low resistance direction and switches the 100-mA tunnel diode to its higher voltage state. See Fig. 4-4 for time relationship waveforms.


SWEEP START PULSE TO R718
PULSER RESET TO Q404
MODE
SYNCHRONIZER CONTROL GATE TO MODE SWITCH,
TRIGGER SENS OR UHF SYNC
R501 100K
D504
Q503
+19V
12K
.02
0.1
100
10K
.001
22
-19V
1V 1ns .25V 50ps UHF SYNC EXT TRIG
SYNCHRONIZER CURRENT TO TD, D485
± SLOPE SELECTOR
INPUT TRIGGER FROM
T512
L510
14T
8T
D515
D516
D517
D518
1μF
39
2K
150
CENTER POSITION OF TRIGGER SENS

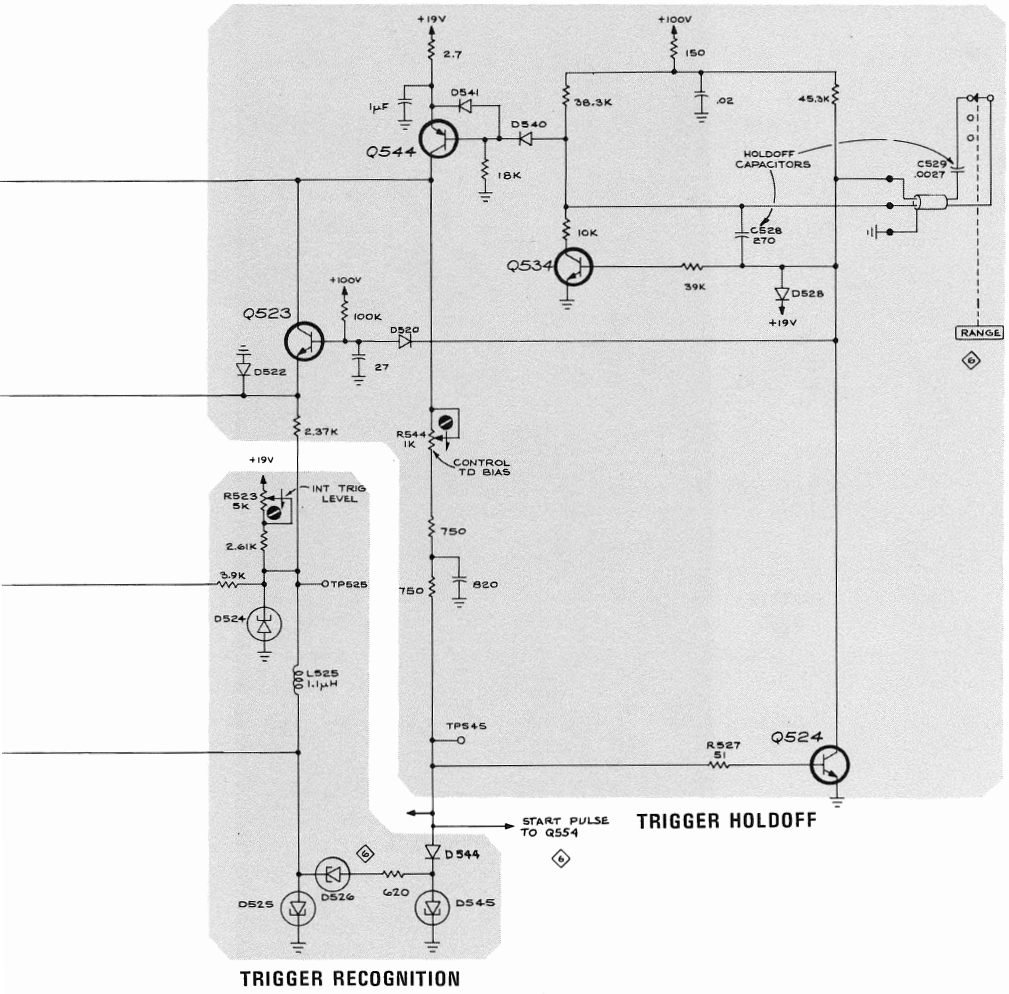


Fig. 4-3. 1S2 Trigger.

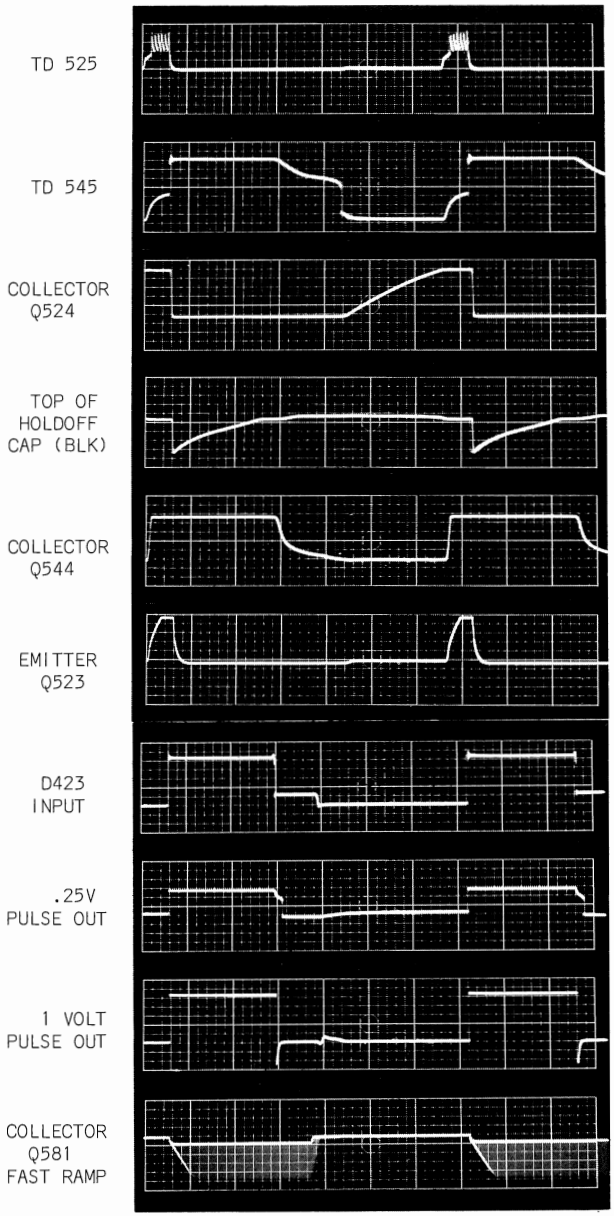


Fig. 4-4. Inside the 1S2.

1S2 TRIGGER CIRCUITS

± SLOPE SELECTOR

The slope selector circuit determines whether the triggering signal will be inverted by transformer T512 or not. When inverted, it is delivered from the secondary winding. By shorting the secondary, the signal may be delivered directly through the primary winding. The circuit prevents having to deliver the triggering signal through switch contacts. When +19 volts is applied to the bottom end of the two 2-k resistors through the 150-ohm resistor, diodes D516 and D517 conduct. Diode D516 conducts through the secondary and diode D517 conducts through the primary (and inductor L519). Because diode D516 is turned on, and because the 1-μF capacitor acts like a short to ground for fast-changing signal components, the secondary may be considered shorted. The primary will then have practically no inductance so the triggering signal will be delivered directly through the conducting diode D517 to the trigger-recognition circuit.

In the EXT TRIG mode, the opposite pair of diodes may be made to conduct by applying -19 volts to the bottom side of the two 2-k resistors. In that mode, diode D515 conducts steadily. It provides a low-impedance signal path to ground for one end of the primary winding of the transformer through the 1-μF capacitor. The secondary then is able to deliver an inverted triggering signal to the input of the trigger-recognition circuit through conducting diode D518.

TRIGGER RECOGNITION

When trigger-recognition tunnel diode D525 and control diode D545 are armed and ready to respond to an incoming triggering signal, both are in their lower voltage state and each is passing nearly its peak point current. When a triggering signal of the right polarity and amplitude appears, the recognition tunnel diode switches to its higher voltage state, makes the control tunnel diode switch to its higher voltage state and starts a fast ramp. The armed and waiting condition prevails only when the EXT TRIG mode is being used.

When either the 0.25-volt pulse or 1-volt pulse is being generated for TDR measurements, the trigger-recognition circuit and holdoff circuits free-run and produce TDR pulses that are automatically delayed and synchronized. In the UHF SYNC mode the fast ramps will also free-run in the absence of an input triggering signal. Fast ramps are started only when the control tunnel diode switches to its higher voltage state. And fast ramps are reset only when the control tunnel diode switches to its lower voltage state. Whether the trigger recognition and holdoff circuits free-run or wait to be triggered depends on whether the trigger-recognition tunnel diode D525 passes more than its peak point current at the end of a holdoff interval.

Bias current for the recognition tunnel diode continually flows through the Int Trig Level pot R523, although part of what flows through R523 is diverted by back diode D524. Part of the bias current may sometimes be diverted through the 3.9-k resistor that is connected to the back diode. In the EXT TRIG mode, when that resistor is connected to the emitter of transistor Q503, the amount of bias current diverted can be controlled by the TRIGGER SENS or UHF SYNC control. It controls the base voltage of emitter follower Q503. With it, enough bias current may be diverted from the recognition tunnel diode to set the bias current less than its peak point value. Most of the bias current is supplied through transistor Q523 at the end of each holdoff interval and only when that current flows may more than the peak point current flow through the recognition tunnel diode.

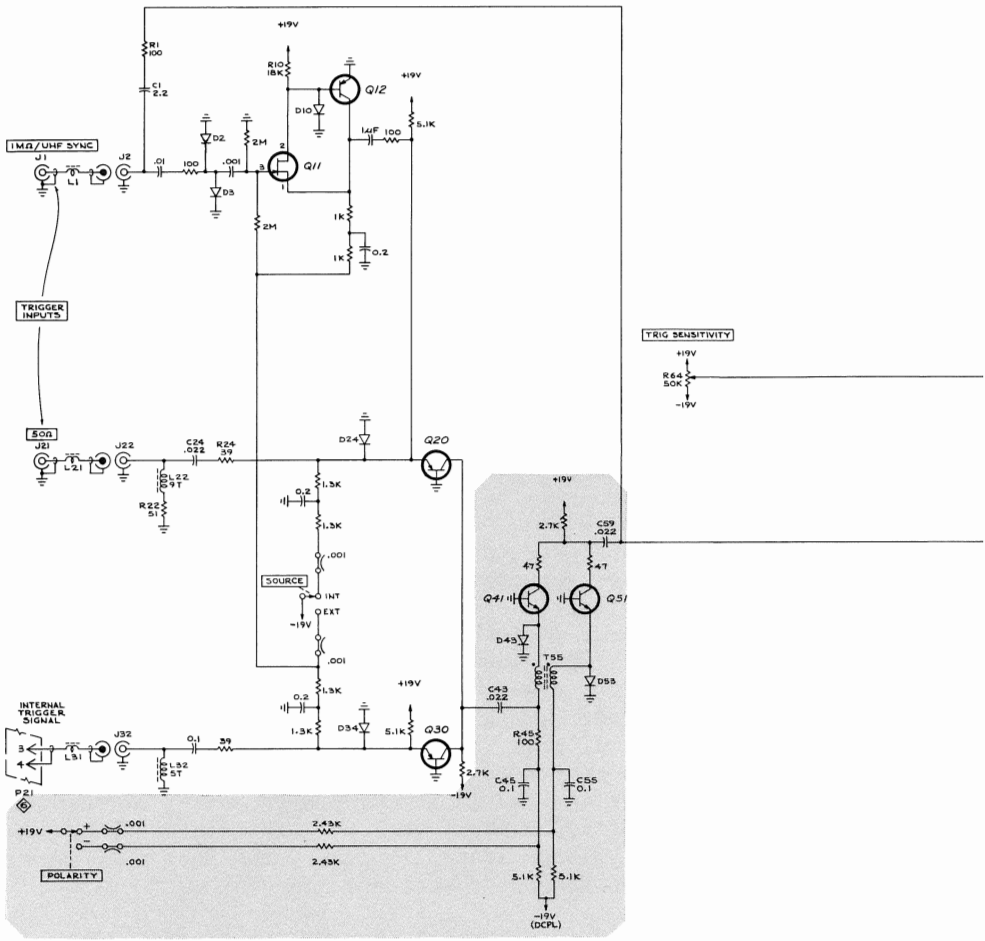
At the end of the holdoff cycle, both transistor Q523 and Q544 turn on at practically the same instant. But the control tunnel diode is not armed at the same instant as the recognition tunnel diode because the 820-pF capacitor at the junction of the two 750-ohm resistors in series with the current path for the control tunnel diode takes a short while to charge. It diverts current from the tunnel diode while charging. Back diode D524 and inductor L525 form a negative resistance oscillator circuit with recognition tunnel diode D525 when sufficient bias current flows to automatically make the tunnel diode switch to its higher voltage state. The circuit oscillates for a few cycles while the control tunnel diode is being armed but immediately is stopped by the holdoff circuit when the control tunnel diode

responds and starts a fast ramp. The frequency of the oscillator depends mostly on the inductance of L525 and the series equivalent resistance of tunnel diode D525 and back diode D524. The frequency is considerably lower than the similar (UHF SYNC) oscillator shown on the 1S2 pulse generators diagram. In the UHF SYNC mode the trigger-recognition oscillator frequency is influenced by the frequency of oscillation of the UHF SYNC oscillator. The frequency should become a subharmonic of the frequency delivered from the UHF SYNC oscillator after a few cycles.

TRIGGER HOLDOFF

When waiting to be triggered, transistor Q523, Q544 and Q534 are on and saturated and transistor Q524 is off. Q524 is off because the combined voltage drop across the control tunnel diode D545 and germanium diode D544 is not great enough to turn it on until the control tunnel diode switches to its higher voltage state. When the control tunnel diode does switch to its higher voltage state, transistor Q524 quickly saturates, turns off Q534 and drives the base of emitter follower Q523 close to zero volts, removing the arming current for the recognition tunnel diode. Both ends of the 270-pF holdoff capacitor suddenly drop 19 volts. Then the voltage on the top side of the capacitor increases as the capacitor charges. Because transistor Q534 was cut off by Q524 saturating the voltage at the junction of diode D540 and the 10-k collector resistor may rise higher than when Q534 is conducting. When the top side of the holdoff capacitor rises high enough, it turns off Q544. That interrupts the bias current supply for the control tunnel diode. The control tunnel diode does not switch to its lower voltage state immediately, however, because the charge in the 820-pF capacitor supplies current for a short while. When it does switch to its lower voltage state, it resets the fast ramp generator and the TDR pulse generator and turns off Q524.

The holdoff capacitor then starts to discharge through the 45.3-k collector resistor, allowing the collector voltage of Q524 to rise. That turns on Q534 again but most of its collector current is diverted by the holdoff capacitor until the holdoff capacitor is nearly discharged. When the bottom end of the holdoff capacitor reaches +19 volts, diode D525 turns on and clamps the voltage at +19.5 volts, stopping the discharge of the holdoff capacitor and allowing the collector current of Q534 to turn on Q544. That ends the holdoff cycle and arms the two tunnel diodes in the trigger-recognition circuit.



±SLOPE SELECTOR AND TRIGGER ISOLATOR

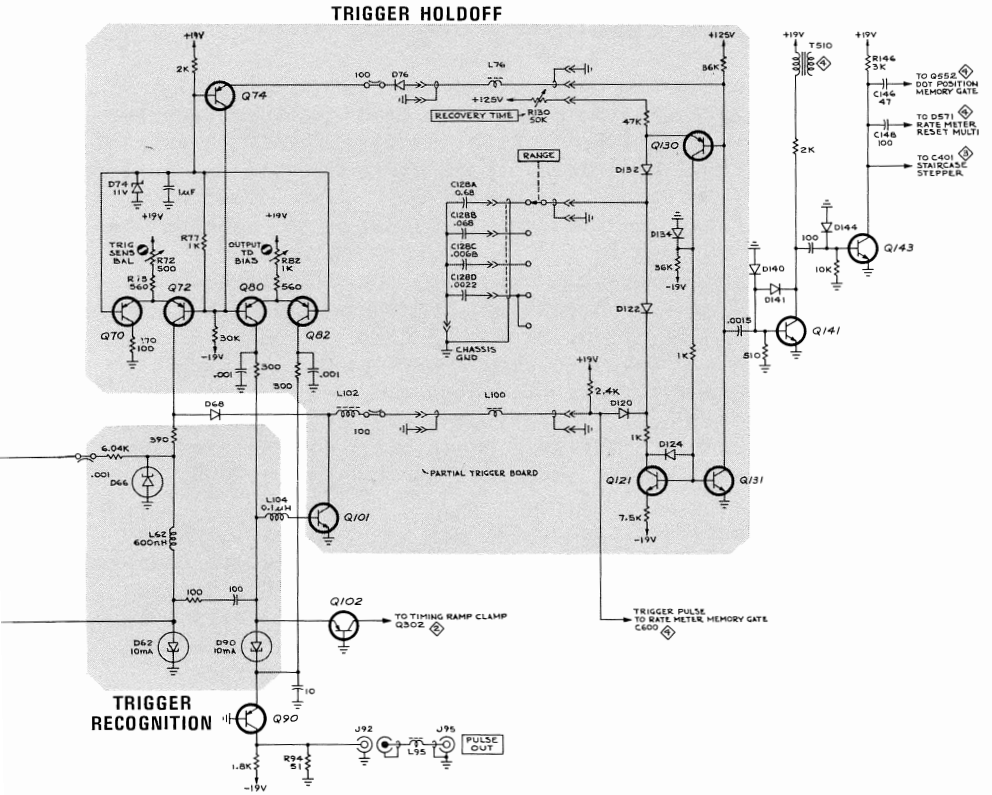


Fig. 4-5. 3T2 Trigger and Holdoff.

3T2 TRIGGER AND HOLDOFF CIRCUITS

input

There are two input connectors for external triggering signals. One is a 50-ohm input and the other is AC-coupled into the parallel resistance of the two 2-M resistors that are connected to the gate of field effect transistor Q11. That input also provides a very short time constant AC-coupled shunt path through C1 and R1 directly to the input of recognition tunnel diode D62 for UHF signals. At that input, conventional 10X 10-megohm probes may be used. The diodes D2 and D5 clip the peaks of tall signals. However, they represent a very high impedance for signals which are no more than about 100 or 200-mV in amplitude. FET Q11 and transistor Q12 form a unity gain noninverting signal follower with low output impedance and high bandwidth.

The gate voltage of FET Q11 is -9.5 volts, set by the divider action of the two 2-M resistors that go between ground and -19 volts when the EXT trigger signal source is selected. FET Q11 operates like a source follower with help from the high open-loop gain provided when its drain drives the base of transistor Q12 and Q12 drives the load at the source of Q11. Current through the 1-k resistors in the source circuit of Q11 is shared by Q11 and Q12 and each stabilizes the share the other gets depending on the beta of Q12 and the current passed by the 18-k drain load resistor.

The output of the signal-follower pair, Q11 and Q12, is AC-coupled through the 1-μF capacitor into the emitter of Q20. Transistor Q20 is turned on for the EXT mode by not diverting the current which flows through the 5.1-k emitter resistor through the two 1.3-k resistors that may go to -19 volts.

In the INT mode, transistor Q30 is turned on and Q20 is turned off by the same SOURCE switch.

± SLOPE SELECTOR and TRIGGER ISOLATOR

The output of Q20 or Q30 is AC-coupled through C45 the 0.022-μF capacitor into the emitter of either Q41 or Q51, depending on the polarity (slope) of the input triggering signal you wish to trigger on. When the plus slope is selected, Q51 is turned off because the divider action of the two resistors in its emitter circuit diverts current from Q51 and turns on diode D53. In that condition, because the top side of the secondary winding of transformer T55 is grounded through diode D53 and because the bottom side is grounded (to AC) through the 0.1-μF capacitor, the secondary is essentially short circuited. With the transformer secondary shorted, its inductance is reduced to practically zero and the signal through the 0.022-μF capacitor appears on the emitter of Q41 unimpeded. At the collector of Q41 the isolated triggering signal is AC-coupled directly to the recognition tunnel diode D62.

When a negative slope is selected, Q41 is turned off and Q51 is turned on. In that condition, the top side of the primary of the transformer is grounded through diode D43 and the voltage induced in the secondary increases and decreases the emitter current of Q51. Its collector then couples an inverted, well isolated signal to the recognition tunnel diode D62.

TRIGGER RECOGNITION

Except for its outputs, the trigger-recognition circuit in the 3T2 operates in essentially the same way as in the 1S1. See the description of the 1S1 trigger recognition circuits for more details (page 118).

When tunnel diode D90 is armed and in its lower voltage state, the current which passes through it also passes through transistor Q90 rather than Q102 because Q90 is a germanium transistor and has a lower emitter-base turn-on voltage than Q102 (which is a silicon transistor). When tunnel diode D90 switches to its higher voltage state, Q102 turns on and diverts part of the current away from D90 and Q90 but not so much that the tunnel diode reverts to its lower voltage state. At that instant a negative step occurs at the collector of Q90 and is fed to the PULSE OUT jack on the front panel. Also at that instant a positive step occurs at the collector of Q102 which starts the timing ramp generator. That positive step is the principle output signal from the trigger holdoff circuit.

At the same instant that diode D90 goes to its higher voltage state, it turns transistor Q101 on hard. The negative-going output step at the collector of Q101 goes to disconnect diode D120 in the trigger holdoff circuit and is fed out to operate the ratemeter memory gate.

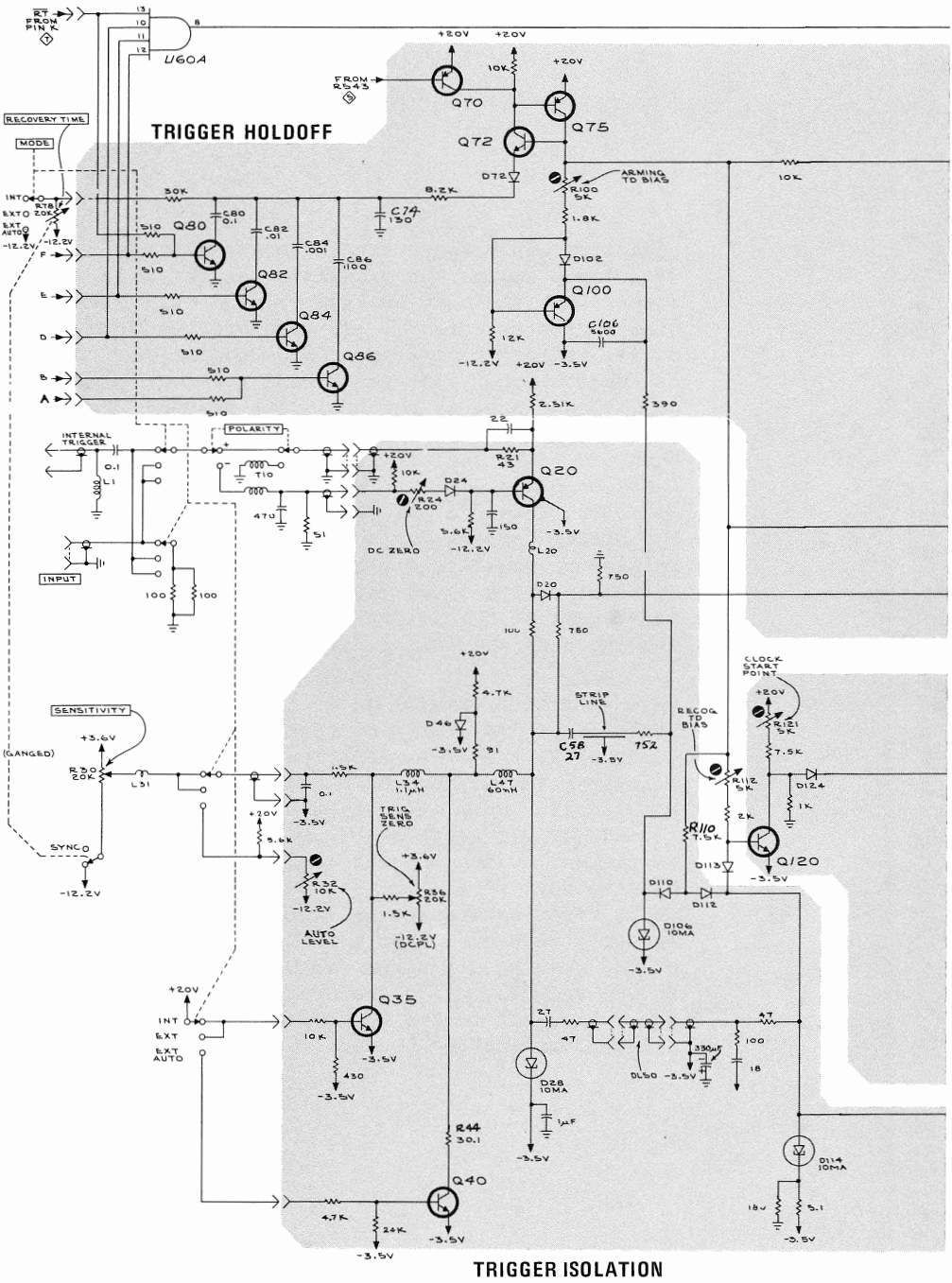
TRIGGER HOLDOFF

In the ready state, when waiting for a triggering pulse, tunnel diode arming transistors Q72 and Q80 are conducting and Q70, Q82 and Q74 are turned off. That is because the bases of Q70, Q82 and Q74 are connected together and are held at +11 volts by zener diode D74. The bases of Q72 and Q80 are about one volt lower than that because of the voltage divider action of the 1-k and 30-k resistors that connect to the bases. Transistor Q74 is not conducting during that time because multivibrator transistors Q130 and Q131 are both conducting and divert current from the emitter of Q74. Transistor Q121 passes a small constant current and, when waiting to be triggered, that current passes through diode D120 and the 2.4-k resistor next to the diode.

The instant a triggering signal is recognized and transistor Q101 turns on, its collector comes down and back biases diode D120. The constant current which flows through Q121 then flows through diode D122 and one of the holdoff capacitors, which then starts to discharge toward ground. Diode D132 will have been back biased by the emitter of Q130, which is close to ground potential. As the holdoff

capacitor discharges, the collector voltage of Q121 diminishes and as the transistor starts to go into saturation, the base voltage of Q131 diminishes and Q131 starts to cut off. By regenerative action multivibrator transistors Q130 and Q131 both cut off. As the collector voltage of Q131 goes up, it turns on Q141 which gates the amplified stopped level of the timing ramp into the horizontal memory capacitor. When Q131 cuts off, it turns on transistor Q74 which turns on Q70 and Q82. That turns off transistors Q72 and Q80. When Q72 and Q80 turn off, they turn off the arming current for both tunnel diodes in the trigger recognition circuit. Tunnel diode D90 then switches to its lower voltage state which ends the first part of the holdoff interval and signals the slewing ramp and timing ramp to reset.

This condition remains until the holdoff capacitor recharges. Its charge current flows through diode D132, the 47-k resistor in series with the recovery-time potentiometer and the RECOVERY TIME pot itself. When it charges above about +11 volts, transistor Q130 starts to turn on because its base is clamped at the emitter level of Q70, which has a base voltage of +11 volts. When Q130 starts to turn on by regenerative action, both Q131 and Q130 suddenly turn on. That turns off Q74. The action of Q74 turning off turns off Q70 and Q82, which turns on Q72 and Q80, which again pass arming current for the two tunnel diodes in readiness for the next trigger, ending the holdoff interval.


TRIGGER HOLDOFF
TRIGGER ISOLATION
RECOVERY TIME
MODE
INT
EXT
EXT AUTO
INTERNAL TRIGGER
POLARITY
INPUT
SENSITIVITY
(GANGED)
SYNC
DC ZERO
TRIG SENS ZERO
AUTO LEVEL
ARMING TD BIAS
CLOCK START POINT
RECOG TD BIAS
STRIP LINE
U60A
Q70
Q72
Q75
Q80
Q82
Q84
Q86
Q100
Q20
Q35
Q40
Q120
D102
D106 10MA
D114 10MA
D28 10MA
+20V
-12.2V
-3.5V
+3.6V

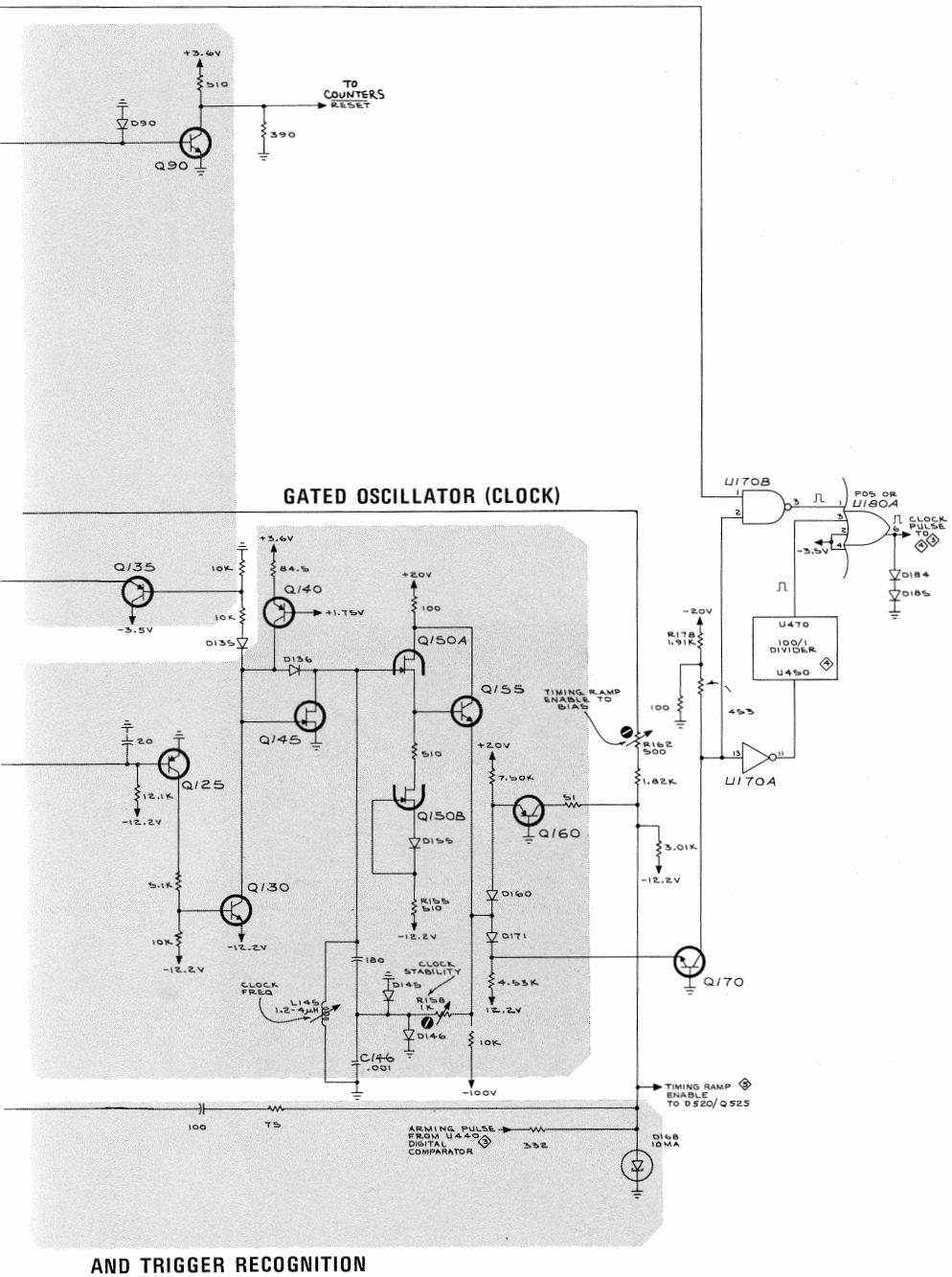
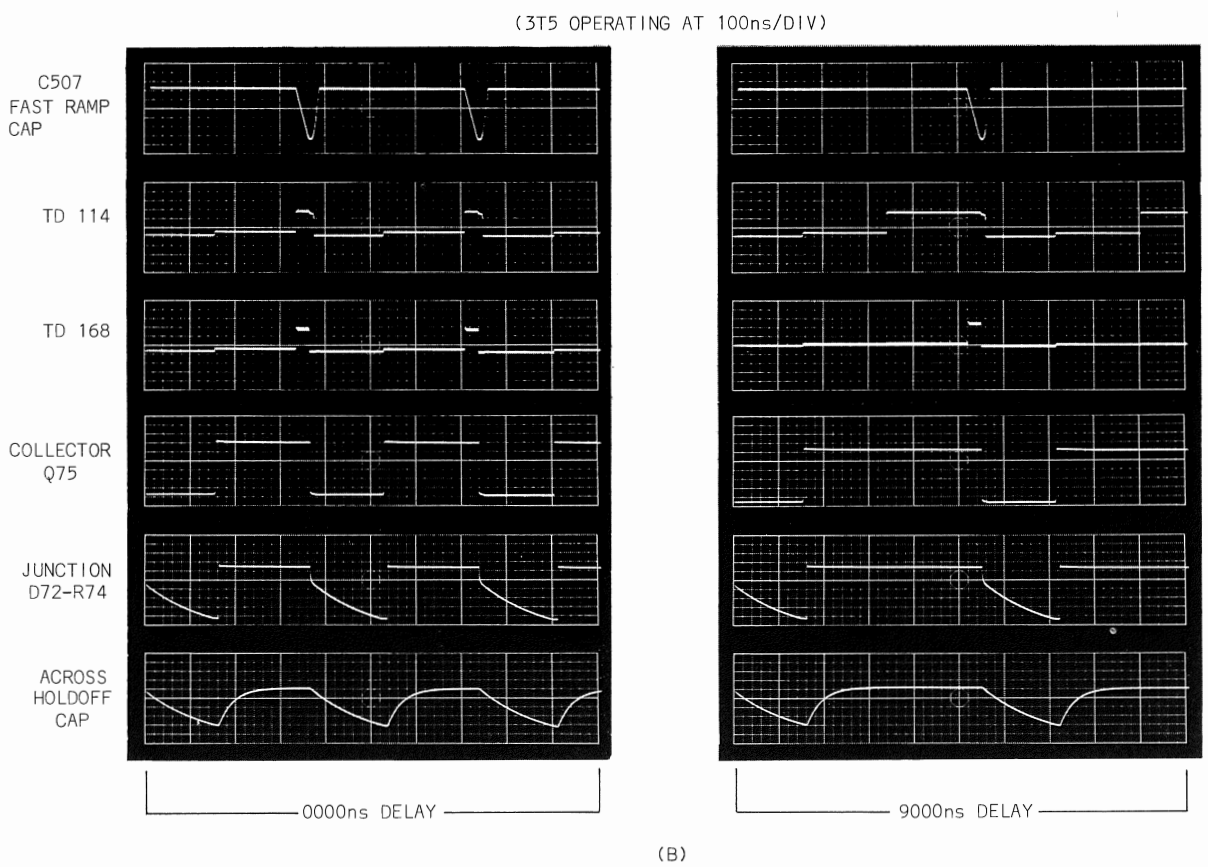


Fig. 4-6. 3T5 Trigger and Clock.


(3T5 OPERATING AT 100ns/DIV)
C507
FAST RAMP
CAP
TD 114
TD 168
COLLECTOR
Q75
JUNCTION
D72-R74
ACROSS
HOLDOFF
CAP
0000ns DELAY
9000ns DELAY

(B)

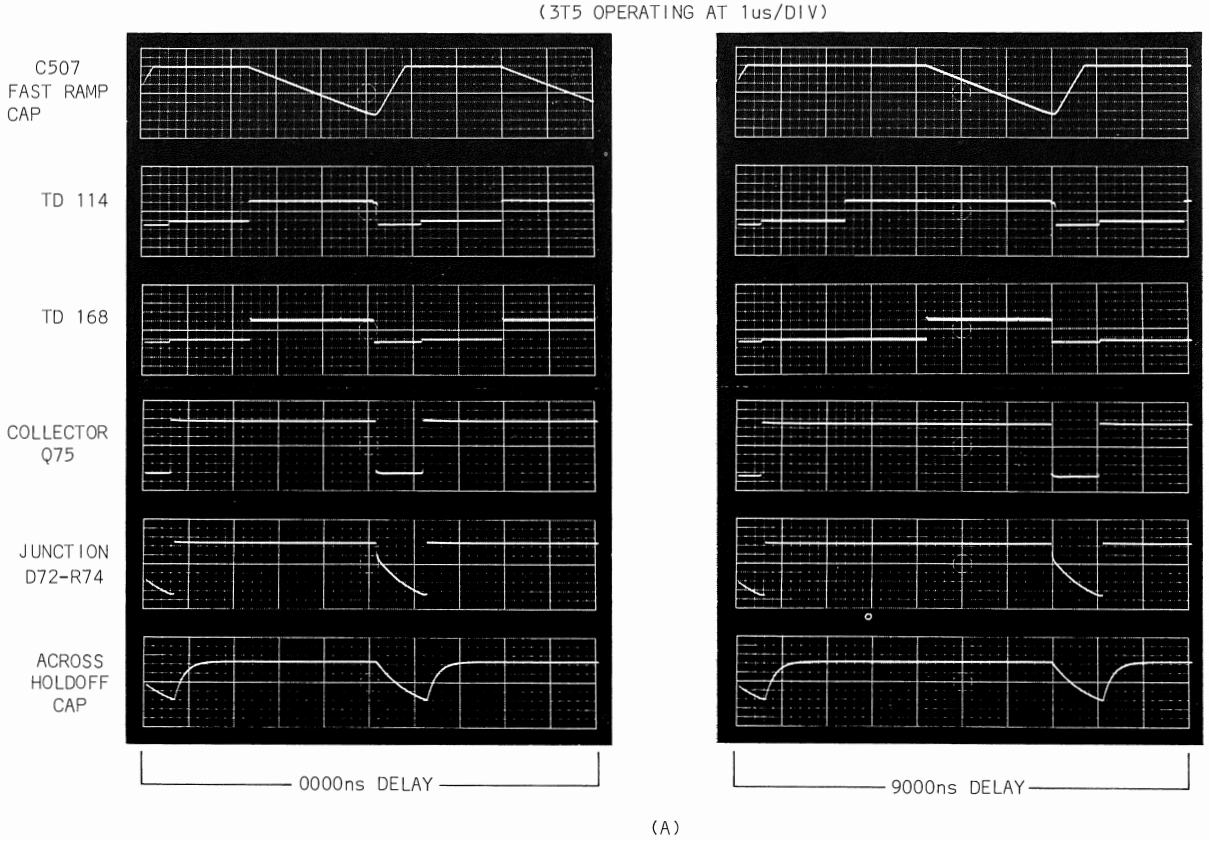


Fig. 4-7. Inside the 3T5. All oscillograms at 5 s/div (549-1A1).

3T5 TRIGGER AND CLOCK CIRCUITS

TRIGGER ISOLATION and RECOGNITION

To minimize trigger kickout, transistor Q20 provides isolation between the source of the input triggering signal and the trigger circuits which recognize and respond to the triggering signal. Its base is operated close to ground potential and is by-passed to ground for fast-changing signal components. The input triggering signal drives the emitter and thereby alters the collector current. When triggering on a negative slope, the fast signal components are inverted by input transformer T10 before being coupled to the emitter and the slower signal components are directly coupled to the base.

There are four tunnel diodes in this circuit, D28, D106, D114 and D168. When waiting for an input triggering signal, all are in their lower voltage state. The one to first respond to the input triggering signal is D28. The one we rely on for an output step signal to start the timing ramps is control tunnel diode D168. That one sometimes responds immediately to drive from tunnel diode D114 and at other times responds later to drive from Q160 in the gated clock circuit, depending on when we cease to divert its arming current. Arming current is diverted through the 332-ohm resistor which connects to the left side of diode D168. The gated clock turns on right after tunnel diode D114 has had a chance to drive control tunnel diode D168 so that whenever D168 is not switched by D114 it will be switched later by the up-going edge of the first cycle from the clock that arrives after D168 is fully armed. That delay will be in 100-ns increments because the period for one cycle of the 10-MHz clock signal is 100 ns.

Tunnel diode D114 cannot respond to a step from the first recognition tunnel diode D28 until it is armed by tunnel diode D106. At the end of a holdoff cycle, when all tunnel diodes are readied to respond to a triggering signal, the arming current for tunnel diode D106 is momentarily diverted by capacitor C106, in the trigger-holdoff circuit, while the capacitor charges. The first recognition tunnel diode D28 may, therefore, respond to several cycles of the triggering signal when first readied before any response is made to its plus steps by either the arming tunnel diode D106 or the second recognition

tunnel diode D114. Notice that in the signal path between the first recognition tunnel diode D28 and the second recognition tunnel diode D114 there is a component labeled DL50. That component is a small 50-ohm coaxial delay cable which provides about 5 ns of delay. In shunt with that path, find the path through C58, R58, D110 and D112. That path has much less delay than 5 ns. It is not a direct signal-coupling path, however, because diodes D110 and D112 are connected anode-to-anode in series and only one conducts at a time.

When the 5600-μF arming-delay capacitor at the collector of Q100 is charged, the arming tunnel diode D106 passes enough current to respond to a plus step from the first recognition tunnel diode D28. Initially, part of the current which flows through tunnel diode D106 flows through D110 and the 7.5-k resistor in series with D110. The rest flows through the 390-ohm resistor, in the trigger-holdoff circuit, that is in series with diode D102. The current which initially flows through tunnel diode D114 flows through diode D113 and no part flows through diode D112. The reason diode D112 is initially off is that the top side of tunnel diode D114 is slightly higher in voltage than the top side of tunnel diode D106 because the cathode of D114 is slightly higher than the cathode of D106. The resistive divider in the cathode circuit of D114 makes the difference.

When tunnel diode D106 steps to its higher voltage state in response to a plus step from the first recognition tunnel diode, the portion of its current which did flow through diode D110 and resistor R110 is switched to pass through diode D112 and tunnel diode D114. That additional current is sufficient to arm tunnel diode D114. Diode D114 thereupon switches to its higher voltage state the instant the first plus step arrives from the first recognition tunnel diode through the 5-ns delay cable. Actually, because of the cable delay, the first plus step to arrive through the cable will be the same one that switched tunnel diode D106 and armed tunnel diode D114.

When tunnel diode D114 switches to its higher voltage state, tunnel diode D168 will also step more positive if a significant portion of its full arming current had not already been diverted through the 332-ohm resistor by a negative voltage at the left end of the resistor. When tunnel diode D114 steps up, it always turns on Q120 in the gated clock circuit. Subsequently, an output from the clock, at the collector of Q160, will cause control tunnel diode D168 to switch to its higher voltage state once it is fully armed if it does not switch when the clock is started.

When ready to respond to an input triggering signal, the current which flows through the first recognition tunnel diode D28 depends on: (1) the current flowing through the trigger isolation transistor Q20, (2) the saturation current of Q35 and (3) the setting of the trigger SENSITIVITY control. (When in the EXT AUTO mode, Q40 substitutes for Q35 and R32 substitutes for the SENSITIVITY control). When the SENSITIVITY control is more than about halfway clockwise, the current through tunnel diode D28 should be greater than its peak point current even in the absence of an input triggering signal, causing the trigger circuits to free-run. The Trig Sens Zero pot R36 affects the point at which the SENSITIVITY control causes the trace to free-run and the threshold should normally be where the dot on the SENSITIVITY knob is between straight up and about 2 o'clock. When the SENSITIVITY control is clockwise from that point or when the SYNC mode is selected, a high-frequency oscillation should occur in the trigger circuit. The frequency is determined primarily by the L/R ratio of the combined series inductance of L34 and L47 and the combined series resistance of tunnel diode D28 and the

saturation resistance of Q35. The negative resistance of the tunnel diode is what makes the circuit oscillate. In the SYNC mode, the frequency is deliberately altered somewhat with the SENSITIVITY control until the oscillator runs at some subharmonic of the triggering frequency. These oscillations occur only during the first moments after trigger holdoff has ended.

Once tunnel diode D106 is armed (C106 charged) and tunnel diode D114 responds to the next plus slope of a cycle of the oscillation, the trigger-holdoff interval begins. Fifty nanoseconds later the current flowing through Q20 is diverted from tunnel diode D28 when transistor Q135 in the trigger-holdoff circuit is turned on. No more tunnel diode oscillations can then occur until the end of the holdoff interval.

In the EXT AUTO trigger mode, Q40 is turned on and Q35 is turned off. The front panel trigger SENSITIVITY control is disconnected and the Auto Level screwdriver adjustment R32 is used instead. This control is normally set just below the free-run threshold so that even a small input triggering signal can be recognized by the first recognition tunnel diode. Although a small signal can be made to switch the recognition tunnel diode to its higher voltage state, the same signal will not normally cause it to switch back to its lower voltage state because of the high peak-to-valley current difference. The hysteresis is therefore reduced by shunting the tunnel diode with L47, R44 and the saturation resistance of Q40.

The adjustable resistors R100, R112 and R162 are placed in series with tunnel diodes D106, D114 and D168 respectively so current may be adjusted for each. The variable resistors permit us to accommodate individual differences in peak point currents of each tunnel diode so each may respond to its proper arming and drive signals and no other.

TRIGGER HOLDOFF

When the trigger-recognition circuit is waiting for an input triggering signal, multivibrator transistors Q72 and Q75 are both on and saturated and all their terminals are close to +20 volts. The +20 volts on the collector of Q75 causes all of the tunnel diodes in the trigger-recognition circuits (except D28) to pass enough current so they may be armed and later switched to a higher voltage state. Prior to this condition, during the time when the last fast ramp from the fast-ramp generator was recovering, the gated clock was being stopped and the clock counters reset to zero. Transistors Q72 and Q75 were both off and none of the tunnel diodes (except D28) was passing enough current to be able to be triggered. As soon as tunnel diode D106, in the trigger-recognition circuit, responds to a plus step from trigger-recognition tunnel diode D28, it turns on Q120, which turns on Q125, which turns on Q130, which turns on Q135, which diverts current from the trigger-recognition tunnel diode. This condition prevails until a fast ramp is generated, runs down a little farther than it needs to go and sends a negative reset step to the base of transistor Q70.

clock and counter reset

At that time, Q70 turns on and it turns off Q75. That turns off Q90, which then resets the clock counters and interrupts the current paths for all tunnel diodes (except D28), switching them to their lower voltage state and clamping the gated clock. The duration of the reset interval is determined by the setting of the RECOVERY TIME control and the size of the capacitor in shunt with C74. Which capacitor shunts C74 depends on whether Q80, Q82, Q84 or Q86 is turned on. As soon as Q72 is turned off, the selected capacitor loses its positive charge through the 30-k resistor in series with R78, the RECOVERY TIME control and the collector-base junction of either Q80, Q82, Q84 or Q86, depending on which transistor base is returned to ground. Current through the capacitors continues when discharged and they start to charge toward the -12.2 volt supply connected at one end of the RECOVERY TIME control.

When Q75 stops conducting, its collector voltage falls to a level about -4 volts below ground, determined by the divider action of the resistors in series with R100 and D90.

While the collector of Q75 is falling, transistor Q100 conducts briefly and discharges C106.

When the voltage across C74 and the selected holdoff capacitor falls below the collector level of Q75 enough so Q72 turns on, both Q72 and Q75 suddenly switch to their saturated state and the circuits are readied to be triggered again.

GATED OSCILLATOR (CLOCK)

In the real-time mode (1 ms/div and more), the 10-MHz clock signal is counted down by a factor of 100 to 1 to a frequency of 100 kHz. At 100 dots/div a 100-kHz clock produces a staircase sweep of 1 ms/div. At sweep rates slower than 1 ms/div, the 100-kHz frequency is divided further so that all sweeps will have the right time-per-dot for 100 dots/div.

In the sequential mode, the purpose of the oscillator is to provide clocked, digital delay for the fast ramps. The fast ramps subsequently initiate sampling-command pulses after additional analog (ramp) delay if desired.

The oscillator is very stable and may be adjusted to precisely 10 MHz with L145. One output is shaped and isolated by transistor Q170 and fed to the counters. Another output is shaped and isolated by transistor Q160 and repeatedly applied to control tunnel diode D168, in the trigger-recognition circuit, every 100 ns. The first time that output is applied to tunnel diode D168 after the diode is fully armed, the tunnel diode steps more positive and starts a timing ramp. Tunnel diode D168 will initiate a fast ramp without the clock if DELAY is set to 0000.

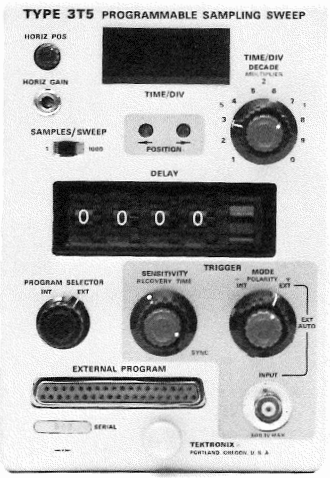
The oscillator circuit involves transistors Q150 and Q155, capacitors C145 and C146, and inductor L145. Field effect transistor Q150A is a source follower which is temperature compensated by Q150B. It drives emitter follower Q155, which drives the 10-MHz tank circuit comprised of C145, C146 and inductor L145. The oscillator will only oscillate, however, when FET Q145, in shunt with the inductor, is cut off. Otherwise, the *Q* of the tank circuit is lowered and the feedback is insufficient to sustain the energy losses.

Transistors Q120, Q125, Q130 and Q135 are off when waiting for a trigger. Q140 is on all the time and passes current for L145 except when FET Q145 is turned off. When FET Q145 is turned off, it unclamps the oscillator.

When tunnel diode D114 in the trigger-recognition circuit goes to its high state, it turns on Q120. That disconnects diode D124, which had been at some positive level dependent on the setting of the Clock Start Point potentiometer R121. After the 20-pF capacitor, at the base of Q125, loses its positive charge, current through the 12.1-k resistor turns on Q125. That turns on Q130, which immediately turns off FET Q145 and interrupts the DC current in the inductor. The magnetic field then collapses, charging C145 and C146 and starting the oscillations. The output starts at zero and goes negative for the first half cycle. The instant the oscillator starts is adjustable and is delayed one-half cycle (50 ns) so the first plus slope will be 100 ns after the second trigger-recognition tunnel diode D114 steps up. Each subsequent plus slope will be 100 ns later.

The Clock Stability control R158 adjusts the amplitude of the feedback so the oscillations don't die out and have the right amplitude. Diodes D160 and D171 steer current to either the emitter of Q160 or the emitter of Q170 and the emitter of Q155 follows the output of the oscillator.

After a fast ramp has been generated, the reset multivibrator in the holdoff circuit turns off the tunnel diodes. That turns off Q120, Q125 and Q130 and allows FET Q145 to stop the oscillator circuit. In the real-time mode, the clock runs for the entire duration of a sweep and is stopped during retrace.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HORIZ GAIN
TIME/DIV
TIME/DIV DECADE
SAMPLES/SWEEP
POSITION
DELAY
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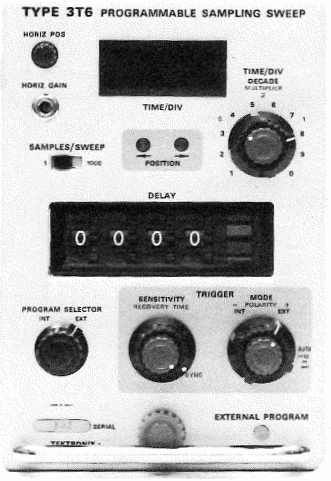
TRIGGER
SENSITIVITY
RECOVERY TIME
MODE
PROGRAM SELECTOR
INT
EXT
EXT AUTO
SYNC
INPUT
EXTERNAL PROGRAM
SERIAL
TEKTRONIX
PORTLAND, OREGON, U. S. A.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HORIZ POS
HORIZ GAIN
TIME/DIV
TIME/DIV DECADE
SAMPLES/SWEEP
POSITION
DELAY
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RECOVERY TIME
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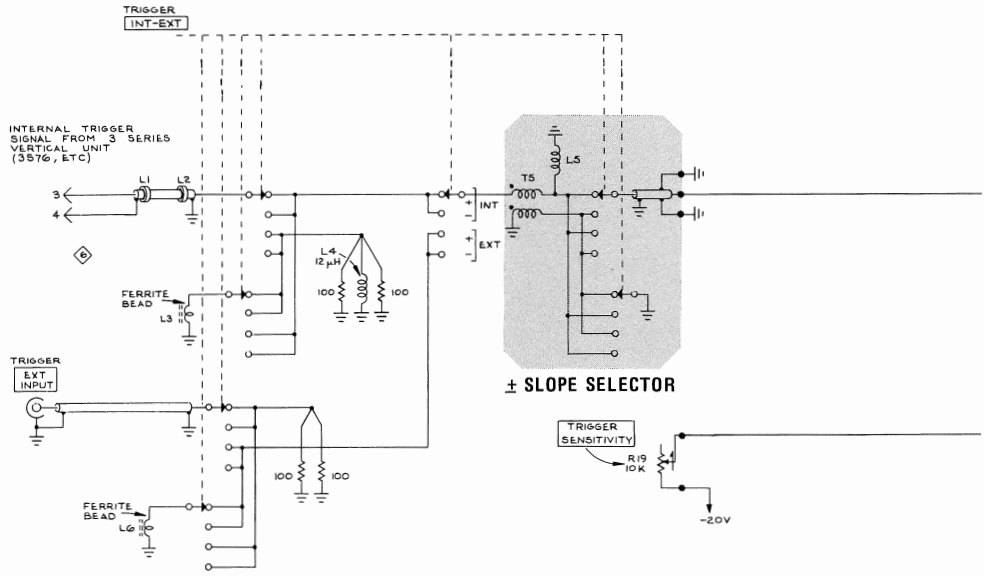
EXT
SYNC
SERIAL
EXTERNAL PROGRAM


TRIGGER
INT-EXT
INTERNAL TRIGGER
SIGNAL FROM 3 SERIES
VERTICAL UNIT
(3S76, ETC)
3
4
L1
L2
6
FERRITE
BEAD
L3
L4
12 μH
100
100
INT
EXT
T5
L5
± SLOPE SELECTOR
TRIGGER
EXT
INPUT
100
100
FERRITE
BEAD
L6
TRIGGER
SENSITIVITY
R19
10K
-20V

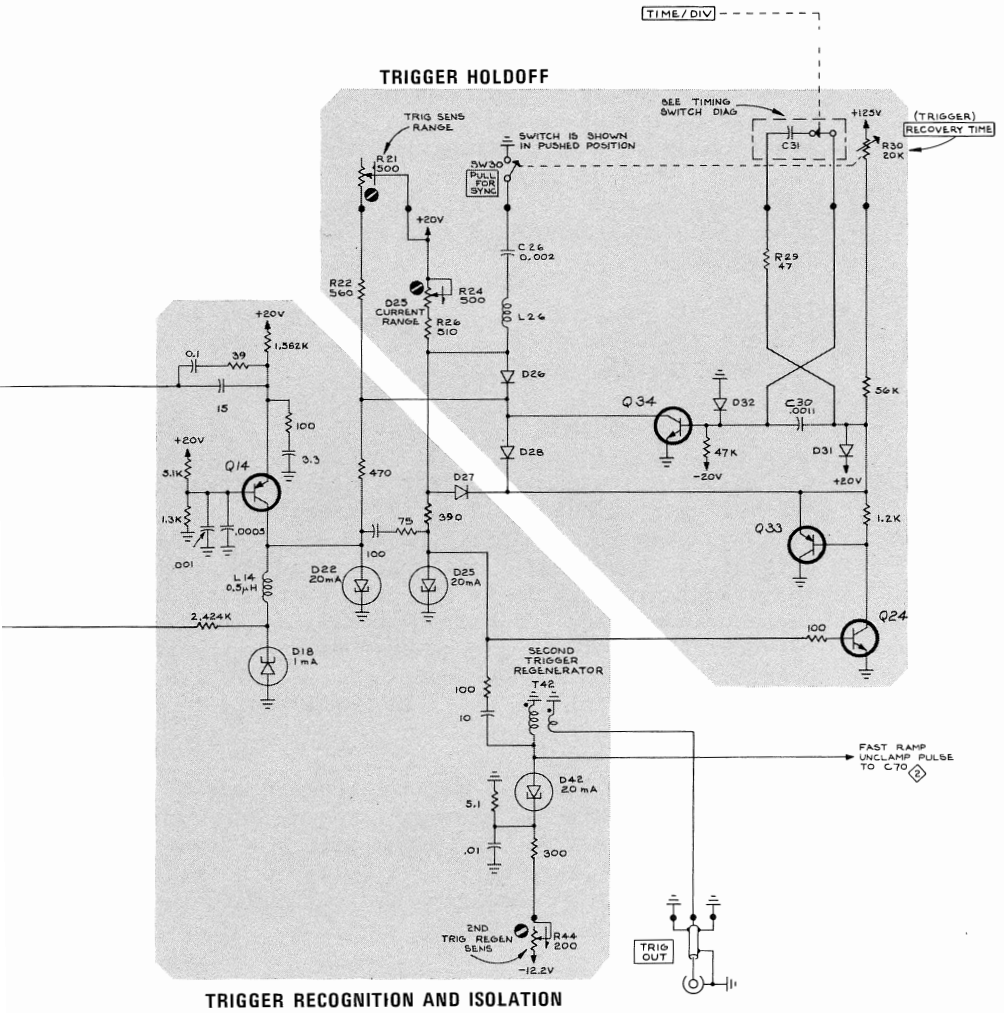


Fig. 4-8. 3T77A Trigger and Holdoff.

3T77A TRIGGER AND HOLDOFF CIRCUITS

± SLOPE SELECTOR

When triggering on the plus slope of an incoming triggering signal, the secondary winding of transformer T5 is shorted. The triggering signal is then fed directly through the primary winding to the emitter of transistor Q14. The primary has practically zero inductance when the secondary is shorted. When triggering on the minus slope, the secondary is used to invert the incoming signal. In that case, the right-hand side of the primary winding is grounded.

The circuit operates in nearly an identical way to the one described for the 1S1. See that description for more details (page 118).

TRIGGER RECOGNITION and ISOLATION

An additional tunnel diode is used, D42. It responds to a plus step from tunnel diode D25 by switching to its higher voltage state, starting a fast ramp and delivering a coincident TRIG OUT signal. Potentiometer R44, 2nd Trig Regen Sens, sets the bias current for diode D42. This control accommodates individual differences in the peak point current of tunnel diodes used for D42. For maximum stability, the control should be set halfway between the peak point current and a lower value threshold where the energy from tunnel diode D25 is barely able to make diode D42 switch.

Potentiometer R24 in the holdoff circuit may be set the same way: Halfway between free-run and won't run. The free-run condition is tested with the front panel TRIGGER SENSITIVITY control R19 fully counterclockwise and the "won't run" condition is tested with the same control set fully clockwise.

When other adjustments are made correctly, the Trig Sens Range pot R21 should be set so the front panel TRIGGER SENSITIVITY control is able to cause a free-run condition when rotated to about the 2 or 3 o'clock position.

TRIGGER HOLDOFF

When waiting for a triggering signal, transistor Q24 is off because tunnel diode D25 is in its lower voltage state. With no current passing through the 1.2-k resistor in the collector circuit of Q24, the base and emitter voltage of Q33 are equal and Q33 is also off. The collector voltage of Q24 is clamped at +20.5 volts by diode D31, which passes current through the 56-k resistor next to it. Transistor Q34 is also held off by the voltage drop across diode D32, which passes current through the 47-k resistor next to it. Under these conditions, diodes D26, D28 and D27 are back biased and adequate arming current for tunnel diodes D22 and D25 should be flowing.

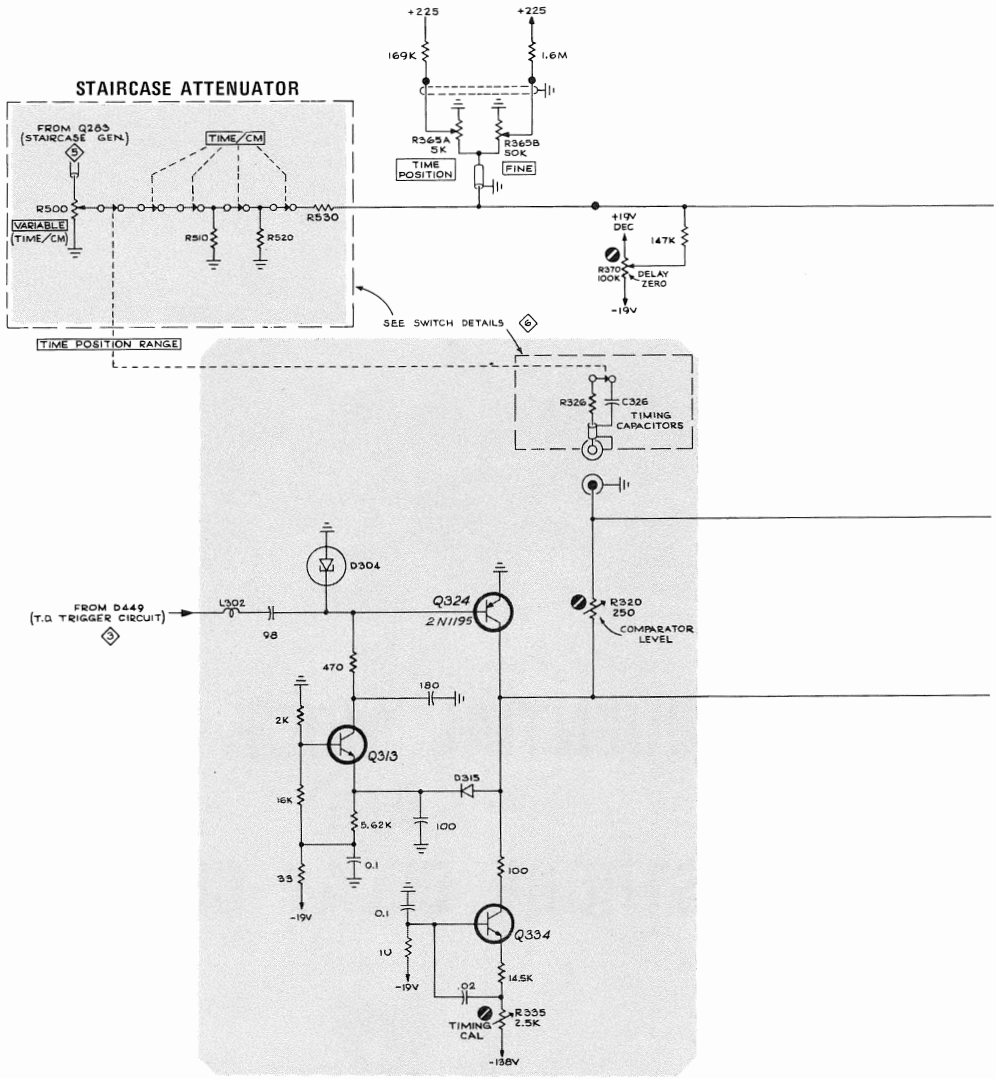
When a triggering signal is recognized and tunnel diode D25 switches to its higher voltage state, transistor Q24 quickly saturates and turns emitter follower Q33 hard on. The holdoff capacitor C30 then quickly discharges. When about half discharged, diodes D27 and D28 conduct and start to divert bias current from the two input tunnel diodes. Soon tunnel diode D25 switches to its lower voltage state and turns off Q24 which turns off Q33, stopping the discharge of the holdoff capacitor.

The holdoff capacitor immediately starts to recharge with current that passes through the 56-k resistor. That diverts current from diode D32 in the base circuit of transistor Q34 and turns Q34 hard on. Transistor Q34 keeps the tunnel diodes switched to their lower voltage state until the holdoff capacitor charges to +20 volts, at which time the run-up is suddenly clamped by diode D31 and the base current of Q34 quickly stops. That ends the holdoff interval and the input tunnel diodes are rearmed.


TYPE 3T77A SAMPLING SWEEP
HORIZONTAL POSITION
VARIABLE
TIME/DIV
GAIN ADJ
μSEC
nSEC
TIME EXPANDER
X10
X1
DOTS PER DIV
10
100
CALIB
UNCAL
TIME POSITION
TRIGGER
SENSITIVITY
MANUAL SCAN
OR EXT ATTEN
SWEEP MODE
MANUAL
NORMAL
SINGLE DISPLAY
RESET
RECOVERY TIME
INT
EXT
PULL
+ EXT SWEEP INPUT
SWEEP OUTPUT
1V/DIV (50 Ω)
TRIG OUT
EXT INPUT
SERIAL
TEKTRONIX
PORTLAND, OREGON, U.S.A.

5

SEQUENTIAL MODE TIMING AND STROBE DELAY CIRCUITS



FAST RAMP GENERATOR

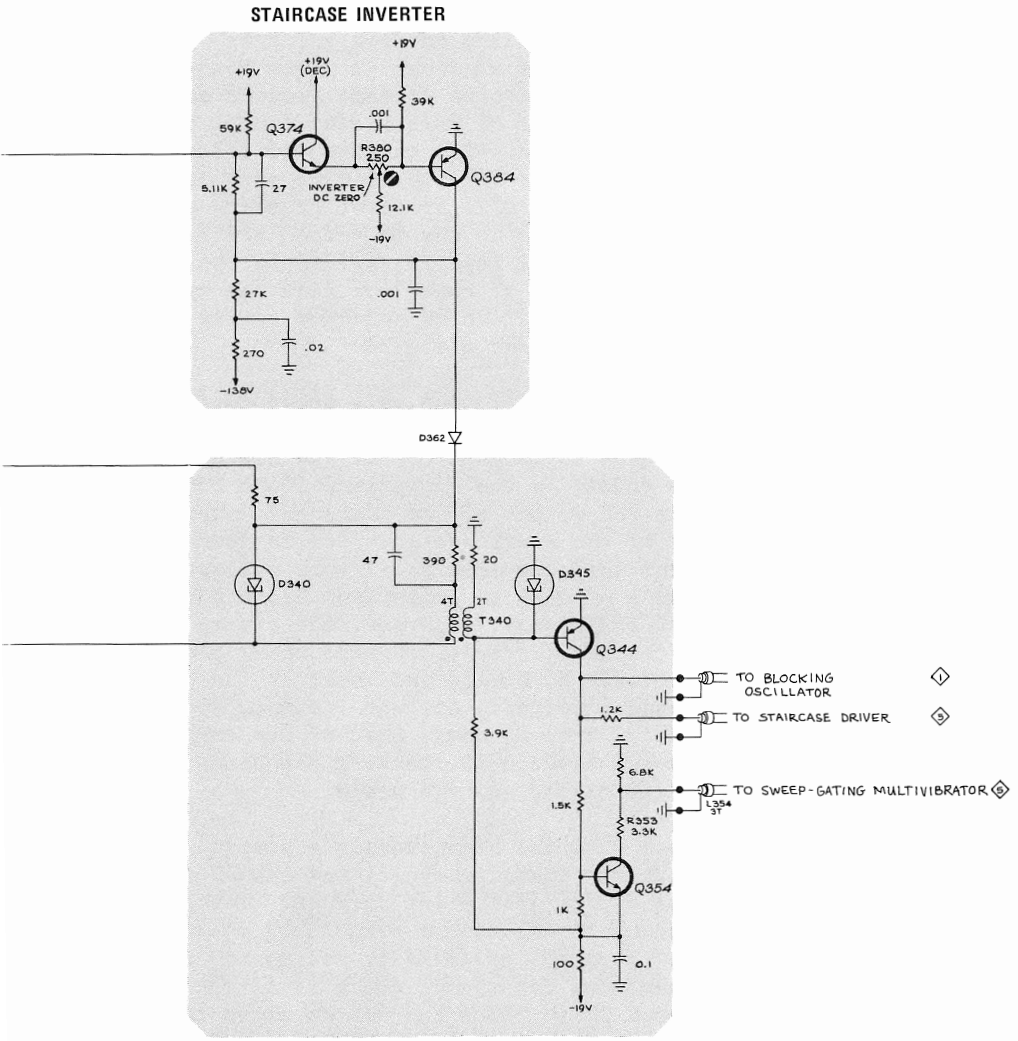


Fig. 5-1. 1S1 Fast Ramp.

1S1 FAST RAMP CIRCUITS

FAST RAMP GENERATOR

When waiting to be triggered, tunnel diode D304 is in its higher voltage state and keeps transistor Q324 turned on hard, passing all the current that flows through constant-current transistor Q334. Transistor Q313 is a voltage-setting emitter follower with a constant base voltage of about -2 volts determined by the 2-k and 16-k resistive voltage divider at the base. The collector current of Q313 biases tunnel diode D304 between its peak point current and valley point current. The emitter voltage of Q313 sets the collector voltage of Q324 at about -2 volts to keep it from saturating so it may be turned off rapidly. When a positive pulse edge is applied to the tunnel diode through the 98-pF capacitor from the trigger circuit, the tunnel diode is switched to its lower voltage state and turns off Q324.

When Q324 is turned off, the only other current path for the current flowing through constant-current transistor Q334 is through one of the timing capacitors (C326) or the comparison diode D362 that connects to the output of the staircase inverter. The output of the staircase inverter is normally always lower than the initial -2 volt collector voltage level of Q324 so comparison diode D362 does not conduct right away. Instead, the timing capacitor charges linearly downward until the voltage across it starts to exceed the level at the output of the staircase inverter. At that instant, diode D362 does conduct. When it does, most of its current goes through tunnel diode D340, causing the diode to switch to its higher voltage state.

Tunnel diode D340 had been passing a portion of the current that was charging the timing capacitor but not as much as its peak point current. The portion it was passing is adjustable with R320, the Comparator Level pot. That pot is normally set so the initial current passed by the tunnel diode is slightly lower than the peak point value but not so close to the threshold that a change in peak point current (sometimes induced by temperature changes) could cause sampling-command pulses to be generated prematurely. Each fast ramp goes down no further than the existing inverted staircase level. But each successive fast ramp goes down further because each new inverted staircase level is lower.

When the first part of the trigger-holdoff interval ends (when depends on the size of the holdoff capacitor selected with the TIME POSITION RANGE switch), a fast negative pulse edge arrives and switches tunnel diode D304 to its higher voltage state. That immediately turns on transistor Q324 and the timing-ramp capacitor discharges. The last portion of the trigger-holdoff interval does not end before the ramp capacitor has had enough time to discharge. The holdoff capacitor is always large enough to assure that.

FAST RAMP COMPARATOR and SAMPLING-COMMAND PULSE GENERATOR

When a down-going fast ramp reaches the level of an inverted stairstep and causes tunnel diode D340 to switch to its higher state, the transition is coupled through transformer T340 to tunnel diode D345, switching it to its higher voltage state. That turns on transistor Q344 very rapidly and Q344 delivers the sampling-command pulses. The sweep-gating multivibrator requires a pulse of opposite polarity so Q354 inverts the pulse that appears at the collector of Q344.

The 20-ohm resistor in series with the secondary winding of transformer T340 shunts most of the current from tunnel diode D345 shortly after each sampling-command pulse is generated so that the tunnel diode switches back to its lower voltage state and turns off Q344. Transistor Q354 then also turns off.

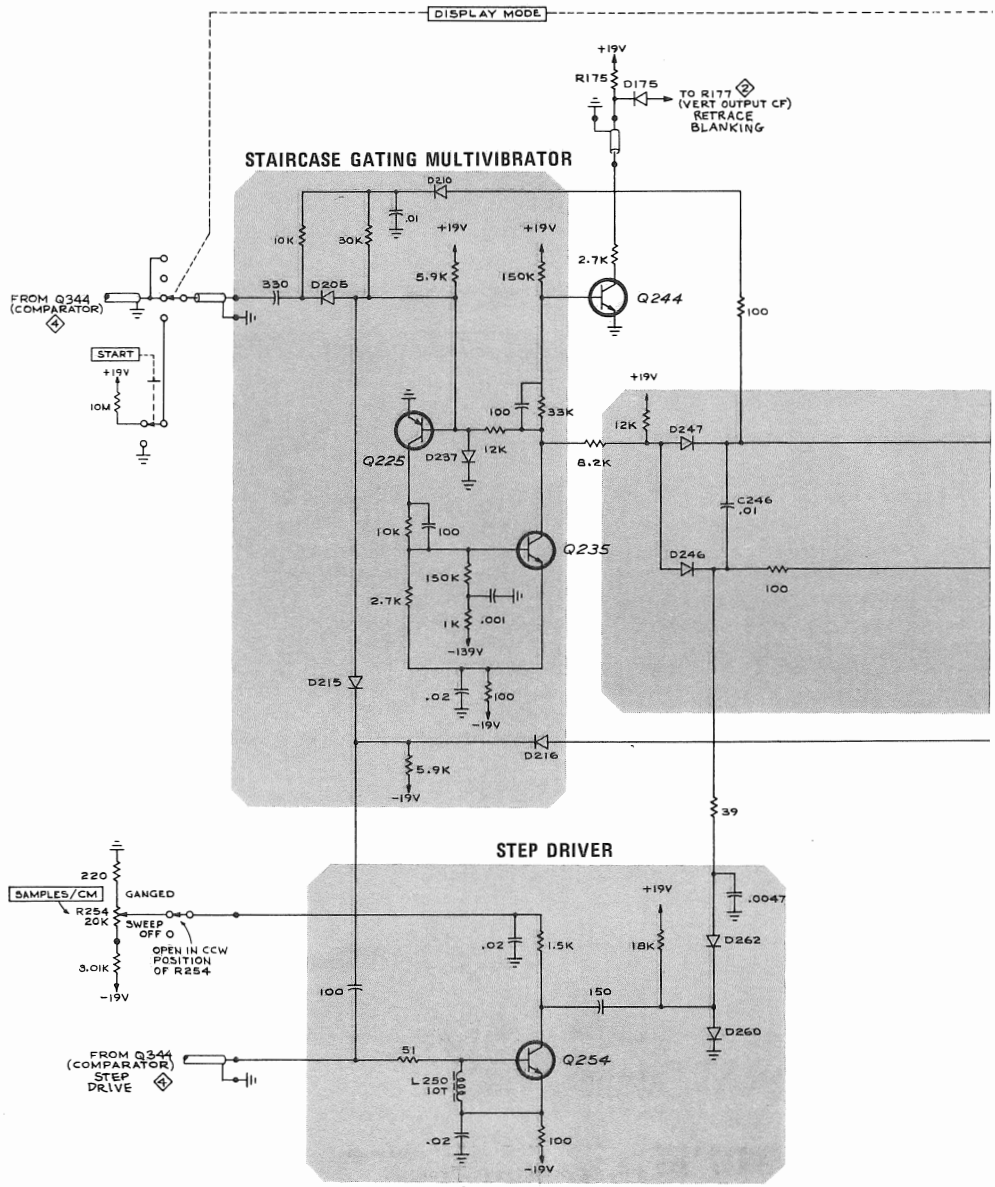
STAIRCASE INVERTER

The staircase inverter is an operational amplifier which receives an attenuated up-going staircase. The staircase starts from a voltage close to zero. The staircase level at the output of the inverter is adjustable with the front panel TIME POSITION controls to introduce offset for the whole staircase. That delays each whole set of strobe pulses and displays portions of the signal otherwise off-screen to the right -- a different time position. The Delay Zero pot R370 and the Inverter DC Zero pot R380 produce a similar shift in the output level and permit the output level to be set correctly. First, the TIME POSITION controls should be set for minimum delay and the Staircase DC Level adjustment set so the staircase starts from zero volts. The Delay Zero adjustment helps keep the output level of the inverter constant for all amounts of staircase attenuation (Time Magnification) when the staircase

input is at zero volts. The Inverter DC Zero adjustment is correctly set when a good compromise is reached between minimizing time-scale nonlinearity and minimizing display delay.

The two inverter adjustments interact with the Comparator Level adjustment R320 in the fast ramp generator circuit. R320 should be set correctly before final adjustments are made to the staircase inverter. When (1) the voltage at the input to the staircase attenuator is zero, (2) the TIME POSITION controls are set for minimum delay and (3) the staircase inverter adjustments set correctly, the output level from the inverter will be practically the same as the beginning level of the linear portion of the fast ramps. That way the comparison diode D362 is able to conduct when the fast ramps first become linear. There is typically a small, abrupt, negative step at the beginning of each fast ramp. It is caused by the voltage drop across the components that are in series with the timing capacitor. Comparison should never be with reference to any portion of the step part of the fast ramp or the time per division will be very nonlinear when delay is minimum.

NOTES


DISPLAY MODE
+19V
R175
D175
TO R177 (VERT OUTPUT CF) RETRACE BLANKING
STAIRCASE GATING MULTIVIBRATOR
D210
.01
10K
30K
+19V
+19V
2.7K
330
D205
5.9K
150K
Q244
100
FROM Q344 (COMPARATOR)
START
+19V
10M
+19V
100
33K
12K
D247
Q225
D237
12K
8.2K
C246 .01
10K
100
Q235
D246
150K
100
2.7K
1K
.001
-139V
D215
.02
100
-19V
D216
5.9K
-19V
39
STEP DRIVER
220
SAMPLES/CM
GANGED
R254 20K
SWEEP OFF 0
OPEN IN CCW POSITION OF R254
3.01K
-19V
+19V
.0047
.02
1.5K
18K
D262
100
150
D260
FROM Q344 (COMPARATOR) STEP DRIVE
51
Q254
L250 10T
.02
100
-19V

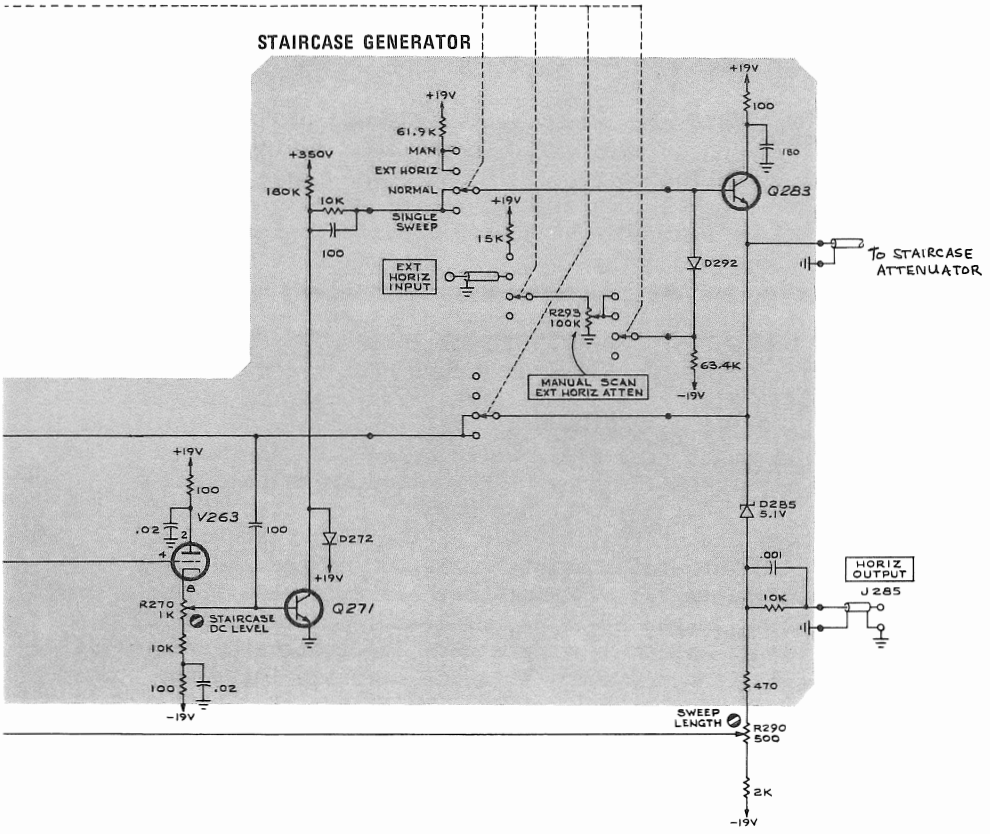


Fig. 5-2. 1S1 Staircase.

1S1 STAIRCASE CIRCUITS

STAIRCASE GATING MULTIVIBRATOR

Multivibrator transistors Q225 and Q235 are either both on or both off. They are on during a sweep and off during retrace. In the NORMAL mode, a negative step may arrive at the base of transistor Q225 via diode D205 and the 330-pF input capacitor whenever a sampling-command pulse is generated if a staircase is ready to be generated. In the SINGLE SWEEP mode, a negative pulse arrives each time the START push button is pressed. During retrace, or before any sampling-command pulses have been generated, both transistors are off. The first negative step that arrives at the base of Q225 turns it on. That turns on transistor Q235, which holds Q225 on when the input step is gone. The collector voltage of Q235 goes well below ground when it conducts, dropping the voltage at the junction of the 12-k resistor and 8.2-k resistor in its collector circuit to a negative value. That back biases diodes D247 and D246 in the staircase generator circuit allowing a staircase to be generated. The staircase reaches an amplitude of about 10 volts before being reset. The staircase at the output jack starts at about -5.1 volts, goes through zero volts, and at about +5.1 volts causes the sweep-gating multivibrator transistors to switch off. The Sweep Length control R290 in the staircase generator circuit determines the precise staircase amplitude required to switch off the multivibrator transistors.

A portion of the 10-volt staircase excursion is available at the arm of the Sweep Length potentiometer. Notice the current path through diode D215 and the two 5.9-k resistors that go to the -19 volt and +19 volt supplies. When the staircase voltage at the arm of the Sweep Length pot goes high enough, current is diverted from diode D215 by current that starts to flow through diode D216 and the junction voltage of the two diodes starts to go up. When the junction goes above ground, it raises the base voltage of transistor Q225 and starts to turn it off. By regenerative action, both Q235 and Q225 then switch off.

During run-up, diode D210 conducts through the 30-k resistor at its cathode and keeps the 0.01-μF capacitor charged to the voltage level of the staircase. That back biases input diode D205 more and more. When the multivibrator switches off, about +10 volts of charge is momentarily stored in the capacitor. During retrace, while the charge is first leaking off, it keeps diode D205 back biased enough to hold off any sampling-command pulses that might otherwise arrive too early and cause the multivibrator to switch back on before the staircase generator had fully recovered.

During retrace, when the multivibrator transistors are off, the retrace blanking transistor Q244 is turned on.

STEP DRIVER

Transistor Q254 is off except when positive-going sampling-command pulses arrive at its base. Its collector-to-ground voltage can be varied from about -16 volts to nearly zero volts by use of the SAMPLES/CM control R254. The same voltage exists across the 150-pF capacitor at the collector. When the transistor is turned on by a sampling-command pulse, the transistor saturates and its collector goes to about -19 volts. That forces the charge that was in the 150-pF capacitor through diode D262 into the 0.0047-μF capacitor at its anode. The 0.0047-μF capacitor thereupon transfers its charge through the 39-ohm resistor into the 0.01-μF Miller capacitor (C246 in the staircase generator circuit) causing a plus voltage step at the top side of C246. As soon as Q254 turns off, the 150-pF capacitor recharges through diode D260 and the 1.5-k resistor in the collector circuit of Q254.

The amplitude of each staircase step is proportional to the charge in the 150-pF capacitor, which is proportional to the voltage across it.

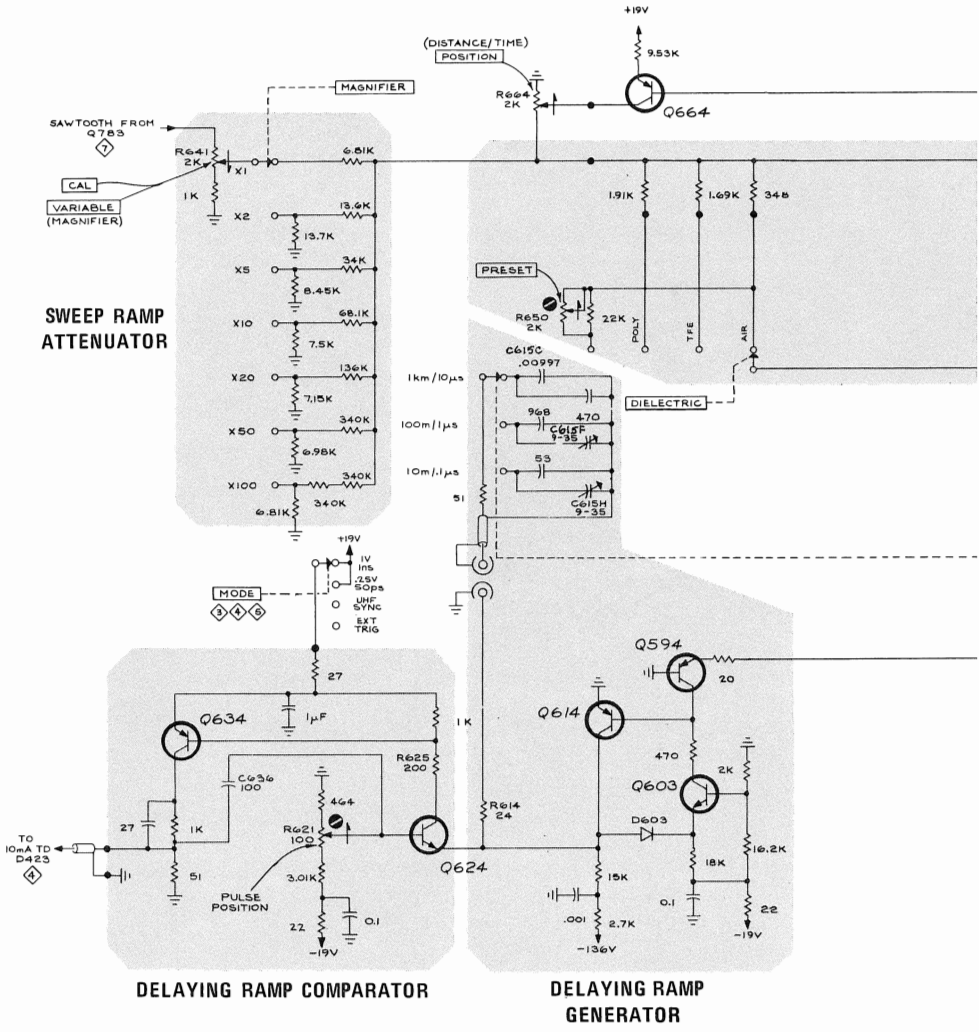
STAIRCASE GENERATOR

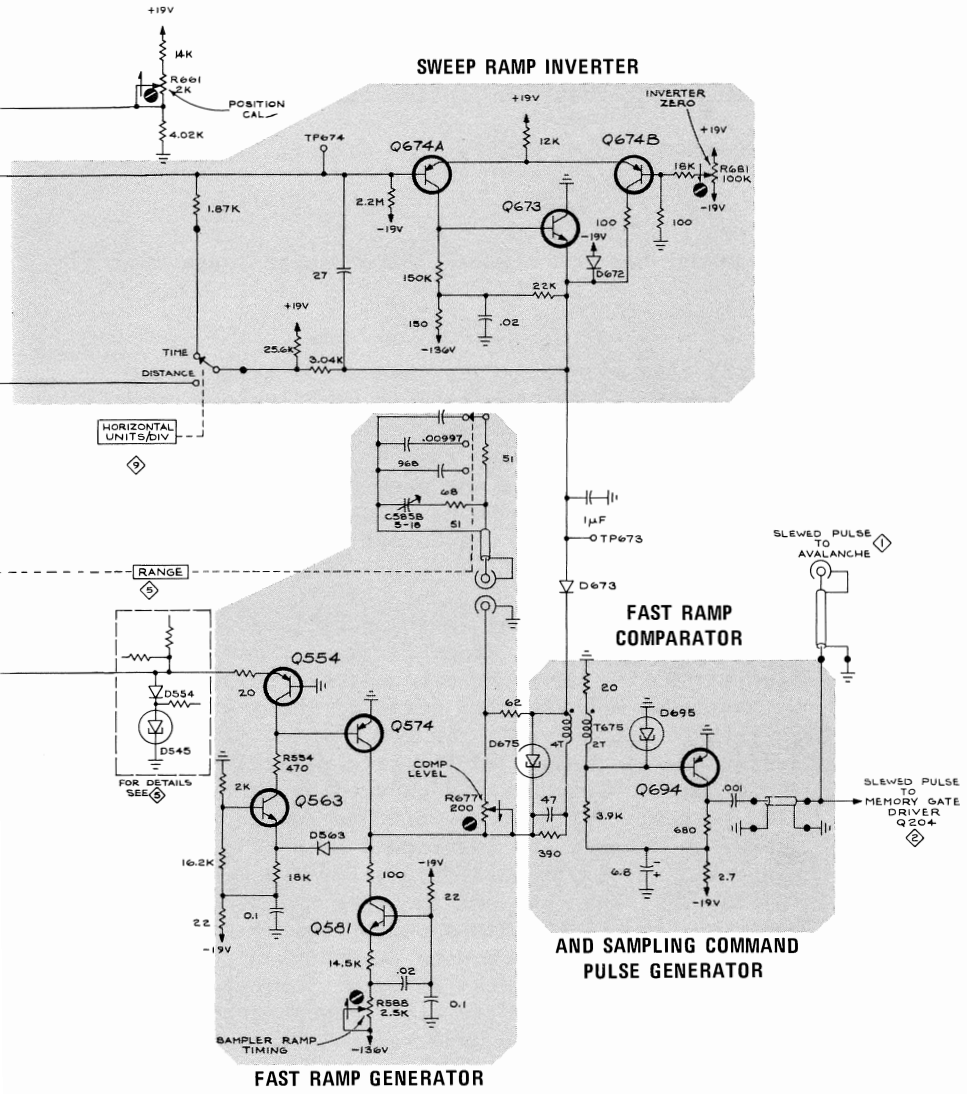
Before each staircase is initiated, diodes D247 and D246 are forward biased by current through the 12-k resistor at their anodes. The voltage across Miller capacitor C246 is therefore practically zero. When Q235 in the staircase gating multivibrator switches on, it drops the voltage at the anodes below ground, in effect disconnecting the diodes. The high open-loop gain of the DC-coupled inverting amplifier, consisting of vacuum tube V263, transistor Q271 and emitter-follower transistor Q283, then forces the grid of V263 to remain at a nearly constant voltage by feedback through the Miller capacitor. A discrete amount of charge is transferred into the Miller capacitor with each step-drive pulse. Because feedback holds the bottom side of the Miller capacitor practically constant, each increase in charge is reflected as an increase in voltage at the top side of the capacitor.

The staircase generator has two outputs. One is tied directly to the emitter of emitter follower Q283 and goes to the staircase attenuator. The staircase voltage at that point runs from ground to about +10.2 volts. The other output is from the bottom side of the 5.1-volt zener diode in the emitter circuit and that staircase runs from about -5.1 volts to about +5.1 volts.

The staircase output emitter follower may be used for the MANUAL SCAN mode or for some EXT HORIZ INPUT scan voltage. In that case, the staircase generator, step driver and staircase gating multivibrator circuits are not used.

NOTES


SWEEP RAMP ATTENUATOR
DELAYING RAMP COMPARATOR
DELAYING RAMP GENERATOR
SAWTOOTH FROM Q783
MAGNIFIER
CAL
VARIABLE (MAGNIFIER)
R641 2K
X1
X2
X5
X10
X20
X50
X100
1K
6.81K
13.6K
13.7K
34K
8.45K
68.1K
7.5K
136K
7.15K
340K
6.98K
340K
340K
6.81K
(DISTANCE/TIME) POSITION
R664 2K
+19V
9.53K
Q664
1.91K
1.69K
348
PRESET
R650 2K
22K
POLY
TFE
AIR
C615C .00997
1km/10μs
100m/1μs
10m/1μs
DIELECTRIC
C615F 9-35
C615H 9-35
51
MODE
1V ins .25V 50ps
UHF SYNC
EXT TRIG
27
Q634
1μF
1K
C636 100
R625 200
464
R621 100
PULSE POSITION
3.01K
22
0.1
-19V
TO 10mA TD D423
R614 24
Q624
Q594
20
Q614
470
2K
Q603
D603
18K
16.2K
15K
.001
2.7K
-136V


SWEEP RAMP INVERTER
FAST RAMP COMPARATOR
AND SAMPLING COMMAND PULSE GENERATOR
FAST RAMP GENERATOR
+19V
14K
R661 2K
POSITION CAL
4.02K
TP674
Q674A
Q674B
INVERTER ZERO
R681 100K
1.87K
2.2M
Q673
D672
27
150K
22K
150
.02
-136V
TIME
DISTANCE
25.6K
3.04K
HORIZONTAL UNITS/DIV
.00997
968
C585B 5-18
51
1µF
TP673
D673
RANGE
SLEWED PULSE TO AVALANCHE
D554
D545
FOR DETAILS SEE
Q554
Q574
Q563
D563
R554 470
COMP LEVEL
R677 200
D675
T675
D695
Q694
SLEWED PULSE TO MEMORY GATE DRIVER Q204
16.2K
18K
100
22
0.1
Q581
14.5K
R588 2.5K
SAMPLER RAMP TIMING
3.9K
680
390
2.7

1S2 FAST RAMP CIRCUITS

FAST RAMP GENERATOR

Except that transistor Q554 is used instead of a tunnel diode to turn Q574 off and on, the fast ramp generator operates in the same way as the one used in the 1S1. See that description for details (page 160).

FAST RAMP COMPARATOR

See description of similar 1S1 circuits (page 161).

SAMPLING-COMMAND PULSE GENERATOR

See description of similar 1S1 circuits (page 161).

SWEEP RAMP INVERTER and SWEEP RAMP ATTENUATORS

The 1S2 uses a linear ramp instead of a staircase for a sweep, so a sweep ramp is used instead of a staircase for the comparator reference level for each fast ramp. As the sweep ramp advances and the horizontal position of the beam advances accordingly, successive sampling-command pulses are increasingly delayed. Attenuating and inverting the sweep ramp is handled the same as if it were a staircase.

The sweep ramp inverter is an operational amplifier with a balanced input stage for good temperature stability. The inverter attenuates the sweep ramp by an amount equal to the ratio of the input resistance and the feedback resistance. The input resistance is changed by the time MAGNIFIER switch. The feedback resistance is changed by the DISTANCE TIME switch. The position of that switch should depend on whether the instrument is used for conventional sampling (TIME) or for TDR measurements (DISTANCE). When the switch is in the DISTANCE position, the DIELECTRIC selector switch provides a choice of four other amounts of feedback resistance. The value of the selected resistor corresponds to the two-way propagation delay time through cables having the type of dielectric material selected.

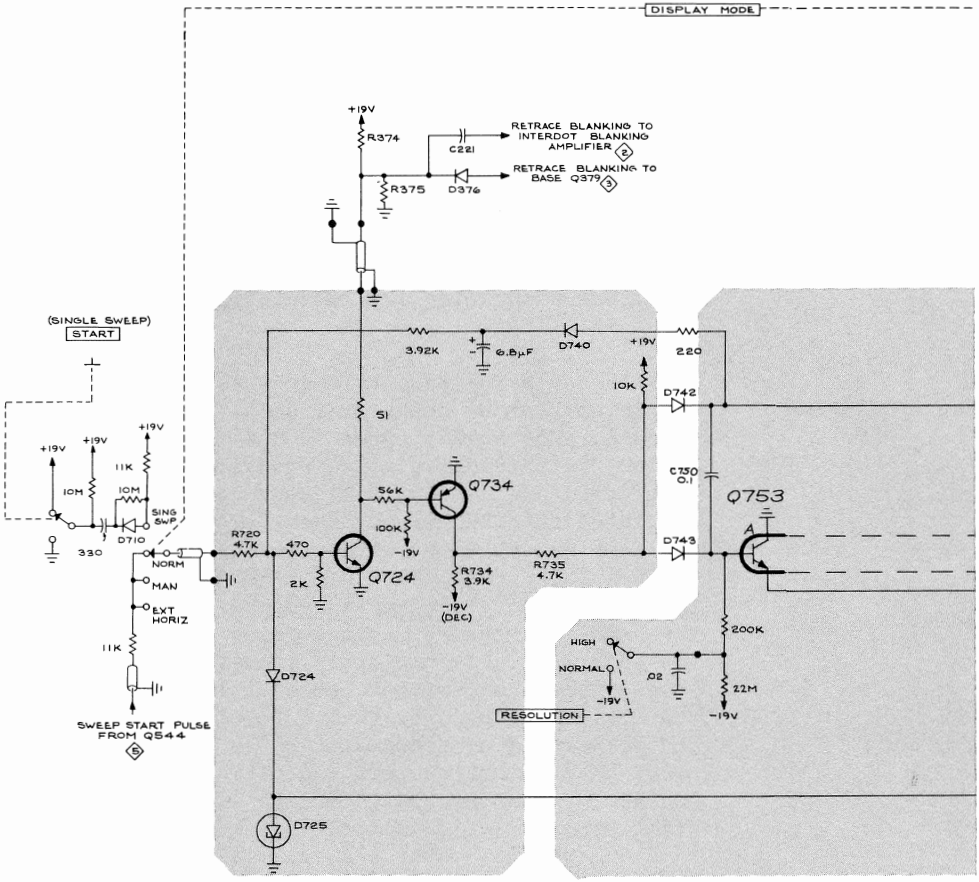
DELAYING RAMP GENERATOR

To initiate and launch a TDR step signal for time domain reflectometry work, the signal must be slightly delayed compared to when each fast ramp is initiated or it will not be possible to sample and display the incident step itself. A delaying ramp is initiated each time a fast ramp is initiated and

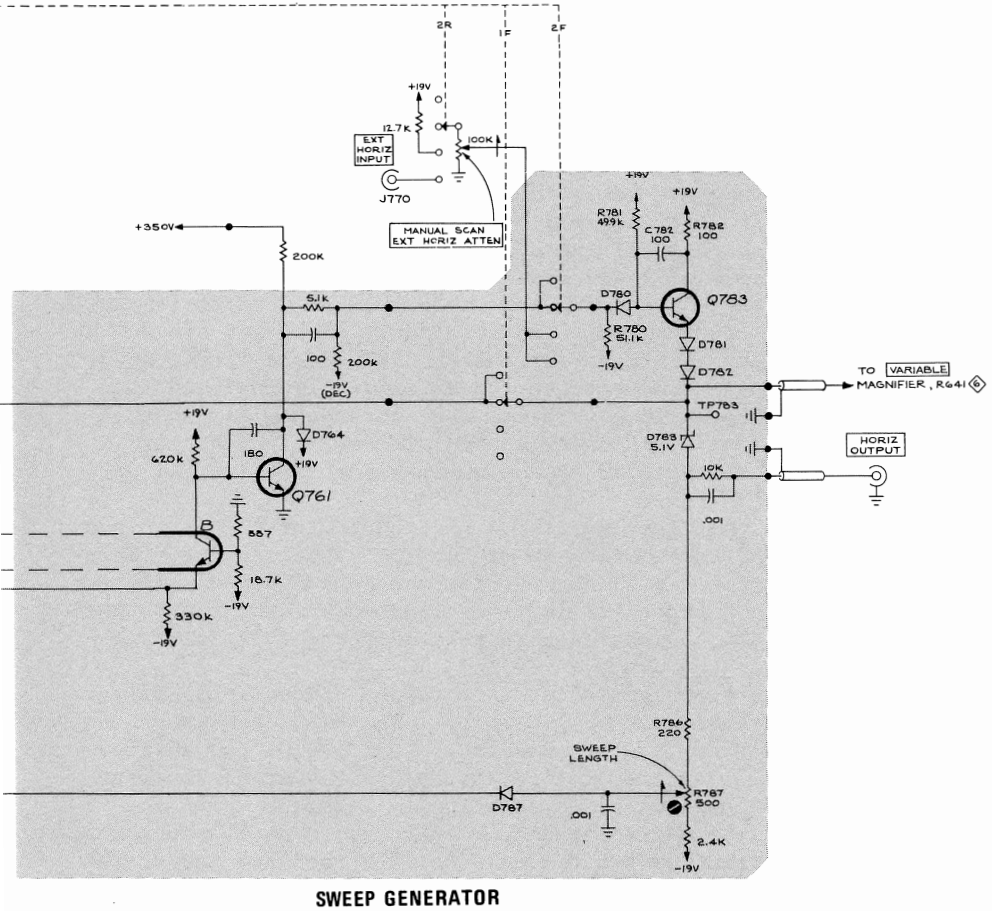
at the same instant. Both ramps, furthermore, have essentially the same slope. In fact, both ramp generators are very similar. The main difference is that there is no constant-current transistor in the delaying ramp generator circuit comparable to constant-current transistor Q581 in the fast ramp generator. A fairly constant current is supplied, however, from the -136 volt supply through the 2.7-k and 15-k resistors in the collector circuit of Q614. When Q614 is cut off, by Q594 turning on and saturating, the constant current is diverted through the 24-ohm resistor and through the selected ramp slope capacitors (C615), charging them in a negative direction. The ramp capacitors discharge through Q614 when a fast ramp reset pulse from the trigger circuit turns on Q614 by turning off Q594. Transistor Q603 is an emitter follower which keeps transistor Q614 from saturating, by clamping its collector at about -2 volts.

DELAYING RAMP COMPARATOR

When the delaying ramp voltage goes down to the level of the emitter of transistor Q624, the transistor turns on and rapidly turns on Q634. By regenerative action, both transistors turn on suddenly and generate a positive step at the collector of Q634. That step initiates the TDR pulse. Each TDR pulse is delayed the same amount with respect to the time each fast ramp is initiated. But that time depends on which of the three ramp slope capacitors have been chosen with the RANGE switch. It also depends on the setting of the base level of comparator transistor Q624. The base level is set with Pulse Position control R621 and determines how far each delaying ramp must go before turning on transistor Q624. After all the other adjustments on this schematic diagram have been correctly made (except C615F and C615H) and with the front panel POSITION control set to 000, the Pulse Position potentiometer R621 may be adjusted. The RANGE should be the longest one, 1 km/10 μs. The control setting will be generally satisfactory as long as the incident step of the applied TDR pulse remains on-screen for all amounts of time magnification from 1X through 100X. The most desirable setting is where the position of the step remains constant at about 1 division from the left-hand side of the screen. Variable capacitors C615F and C615H are then adjusted for a comparable condition using the other two ranges. See Fig. 4-4 for time relationships.


DISPLAY MODE
+19V
R374
C221
RETRACE BLANKING TO INTERDOT BLANKING AMPLIFIER 2
R375
D376
RETRACE BLANKING TO BASE Q379 3
(SINGLE SWEEP)
START
3.92K
0.8µF
D740
+19V
220
10K
D742
51
C730 0.1
Q753
56K
Q734
100K
R720 4.7K
470
Q724
2K
R734 3.9K
-19V (DEC)
R735 4.7K
D743
11K
10M
10M
SING SWP
D710
330
NORM
MAN
EXT HORIZ
11K
SWEEP START PULSE FROM Q544 5
D724
200K
HIGH
NORMAL
.02
22M
-19V
RESOLUTION
D725

RAMP GATING



SWEEP GENERATOR

Fig. 5-4. 1S2 Sweep Generator.

1S2 SWEEP GENERATOR CIRCUITS

RAMP GATING

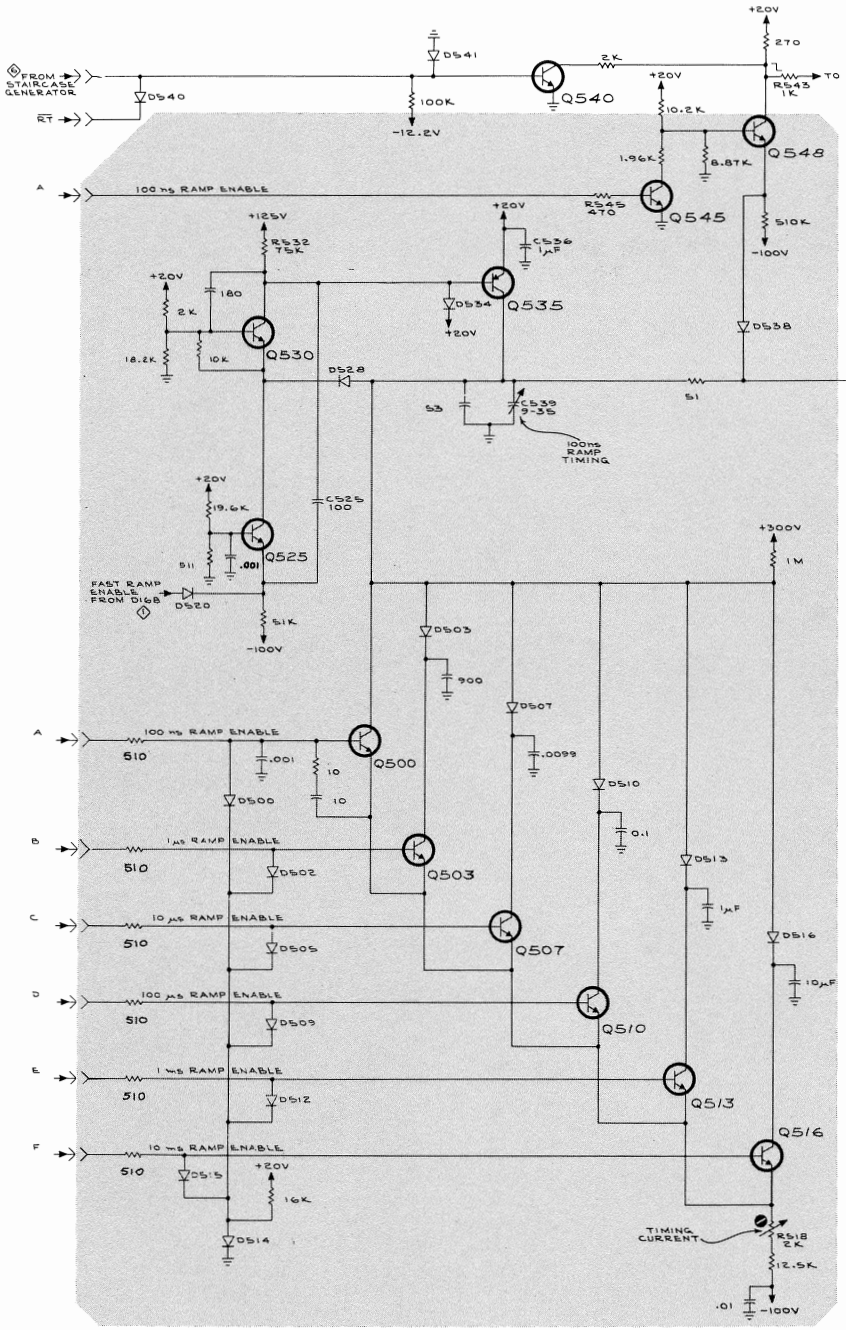
When waiting to be triggered, the two transistors in the ramp gating circuit are both on. Tunnel diode D725, being in its higher voltage state, turns on Q724, which turns on Q734. The tunnel diode bias current flows through the 4.7-k resistor in series with the input as long as a positive (+19) voltage is applied at the input. In the middle of a fast ramp holdoff cycle, that voltage goes down close to ground and makes the tunnel diode switch to its lower voltage state, which turns off Q724 and Q734. That drops the voltage at the left-hand side of disconnect diodes D742 and D743 and starts the sweep ramp. After a sweep has run up to about +10 volts (+5 volts at the horizontal output jack), the wiper arm on the Sweep Length potentiometer R787 goes a little above ground and switches tunnel diode D725 back to its higher voltage state. That turns on Q724 and Q734 again, ends the sweep and discharges the Miller capacitor C750 in the sweep-generator circuit.

In the meantime, the 6.8-μF capacitor next to diode D740 has charged to +10 volts. That capacitor then supplies bias current for the tunnel diode while the sweep generator is recovering and allows the tunnel diode to ignore start pulses during that interval.

SWEEP GENERATOR

The sweep generator is a fairly conventional Miller integrator ramp generator. The high open-loop voltage gain of transistors Q753, Q761 and emitter follower transistor Q783 hold the voltage level at the base of Q753A practically constant while the 0.1-μF Miller capacitor charges. Most of the charge current passes through the 22-M resistor and/or the 200-k resistor in the base circuit of Q753A. The 5.1-volt zener diode in series with the emitter load for Q783 sets the output sweep start level at about -5 volts so that a 10-volt sweep goes equal amounts above and below ground.

NOTES



TIMING RAMP GENERATOR

B1

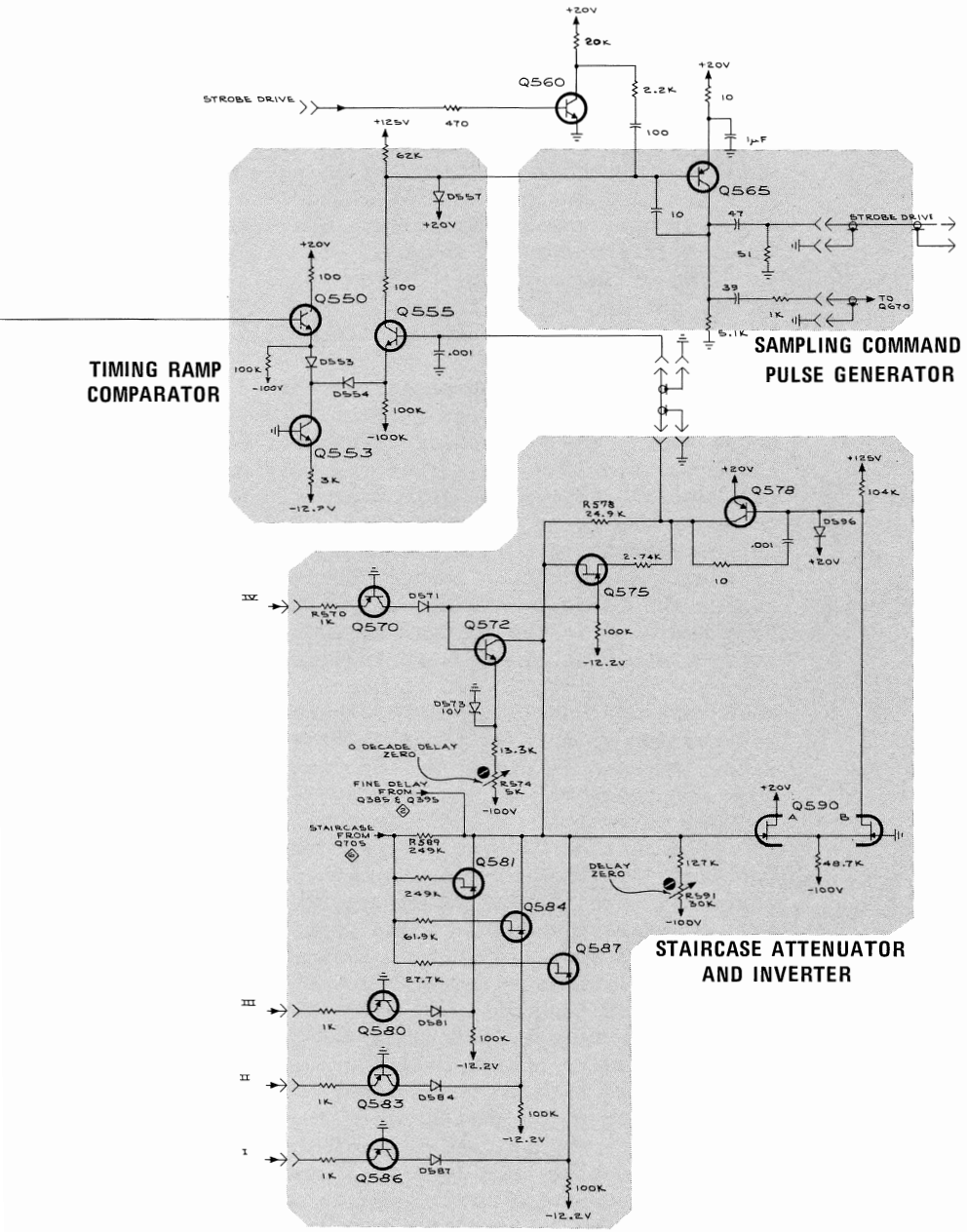


Fig. 5-5. 3T5 Timing Ramp and Staircase Inverter Amp.

3T5 TIMING RAMP AND STAIRCASE INVERTER AMPS CIRCUITS

TIMING RAMP GENERATOR

In the 3T5 there is a choice of one of six different timing ramps with slopes that differ from each other by decade steps. The ramp slope capacitors are selected by turning on one of six constant-current transistors Q500, Q503, Q507, Q510, Q513 or Q516. Which one of these is turned on is determined by what time per division has been selected from the front panel or programmed externally. The selection is decoded internally and about +1 volt is applied to the base of the appropriate transistor. The inputs to all but one of the transistors is held close to +0.5 volts by current through diode D514.

Transistor Q525 is a constant-current (2 mA) supply for Q530, except when its current is diverted by diode D520. The emitter of transistor Q530 stays close to the +18 volts set by the voltage divider at its base and clamps the collector of transistor Q535 at about +18 volts, through diode D528, to keep Q535 out of saturation. Transistor Q535 is turned on hard by a portion of the collector current of Q530 and passes the constant timing current which flows through R518 and R519 in the emitter circuit of the selected constant-current timing ramp transistor.

When control tunnel diode D168 in the trigger-recognition circuit switches to its higher voltage state, current is diverted from transistor Q525 and Q530 and turns off Q535. The fast edge of the plus step at the emitter of Q525 is coupled through the 100-pF capacitor C525 and helps turn off Q535 rapidly. The instant Q535 is turned off the constant current it was passing flows through one of the timing capacitors and a linear fast ramp starts running down from +18 volts. Each ramp continues down until it goes slightly below the level on the emitter of emitter follower Q548 at which time current is diverted through diode D538 and Q548 and produces a negative swing at the collector of Q548. That signal is fed back to the trigger holdoff multivibrator which switches off and turns off tunnel diode D168 in the trigger-recognition circuit. Tunnel diode D168 then ceases to divert current from transistors Q525 and Q530, turning Q535 back on and ending the ramp. The timing capacitor then quickly recharges to the +18 volts at the collector of Q535 and by the time the reset interval has expired, a ramp is ready to run down again.

The voltage level at the emitter of Q548 depends on whether Q545 is on or off. When turned off, the base level of Q548 is determined primarily by the divider action of the two resistors in its base circuit, which go to ground and to +20 volts. That sets the emitter at about +8 volts. When transistor Q545 is turned on, the emitter level resets at about +1.5 volts. Transistor Q545 is only turned on when the fastest fast ramp (100 ns) is selected. That allows the ramp to run from +18 volts to +1.5 volts instead of +18 volts to +8 volts. The extra length is needed because 0.1-ns, 1.0-ns and 10-ns delay increments are achieved using that ramp for the top decade of 100 ps, 200 ps and 500 ps per division. Delay increments of 100 ns and higher are achieved using the 10-MHz clock and digital counter.

In the real-time mode, when the fast ramps are not used, the negative reset step needed at the collector of Q548 is supplied by a plus step at the base of Q540 from the staircase multivibrator at the completion of a sweep.

TIMING RAMP COMPARATOR and SAMPLING-COMMAND PULSE GENERATOR

Before each fast ramp is completed and reset, it must initiate a sampling-command pulse at the instant when it crosses a horizontal dot-position reference level -- usually an attenuated and inverted staircase level. Transistors Q550, Q553 and Q555 are the active elements in the comparator. Q555 is an emitter follower coupled to the output of the staircase attenuator and inverter circuit. Q550 is also an emitter follower at all times when its emitter is at a higher level than that of Q555. It passes a constant (4 mA) current set by Q553. The emitter of Q550 follows the down-going fast ramp applied at its base until its emitter and diode D553 start to go below the level of the emitter of Q555. At that instant, additional current switches into Q555, which suddenly turns on Q565 and generates a sampling-command pulse.

STAIRCASE ATTENUATOR and INVERTER

A positive staircase is applied from the staircase generator circuit to one side of the 249-k resistor R589, which is at the input to Q590. Balanced FET Q590 and transistor Q578 are part of an operational amplifier. The feedback resistor is R578. In shunt with the input resistor are three resistors each in series with the drains of field effect transistors Q581, Q584 and Q587. In shunt with the feedback resistor is FET Q575 with a 2.74-k resistor in series with it. When any of the field-effect transistors is turned on, it has a resistance of approximately 30 ohms. When turned off, they are practically an open circuit.

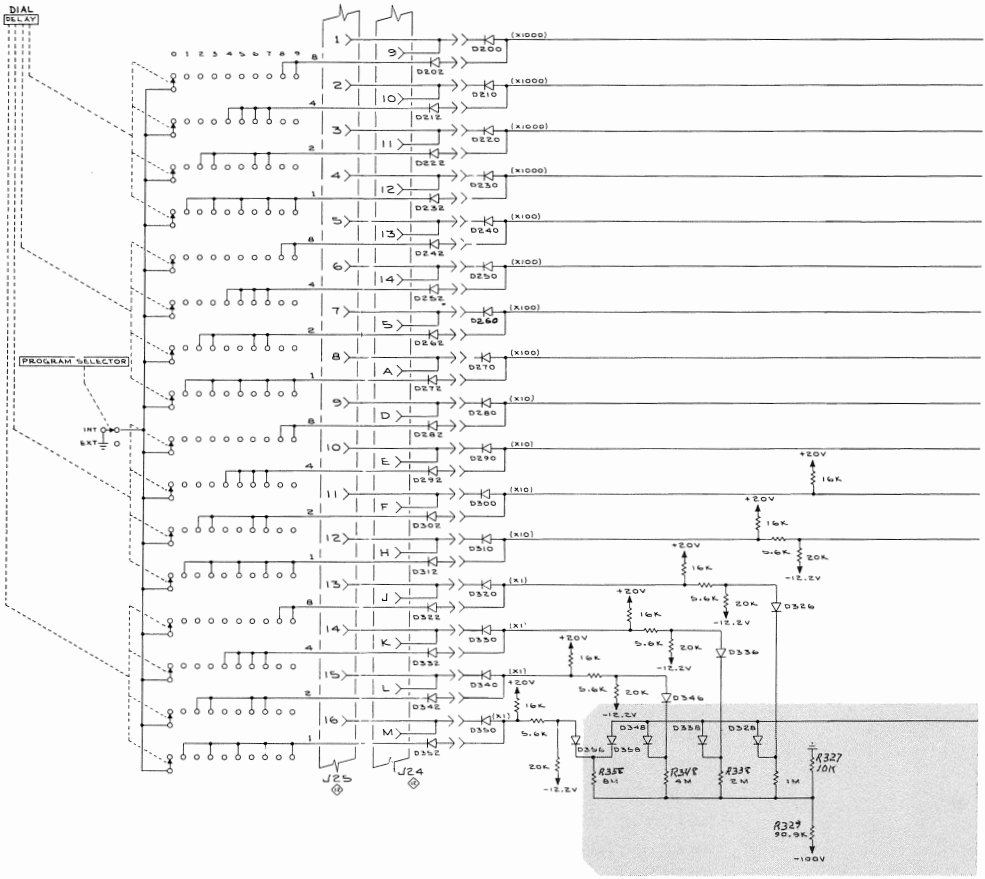
By turning on the FET that is in shunt with the feedback resistor, the equivalent resistance is lowered by a factor of ten, reducing the gain by a factor of ten. This attenuates the inverted staircase by an additional factor of ten and reduces the time per division by the same factor. Shunting the input resistor increases the time per division. The time per division increases by a factor of 2X when Q581 turns on. When Q584 turns on, the factor is 5X and when Q587 is on, the factor is 10X. Time magnification of 1X, 2X, 5X, 20X, 50X and 100X may be achieved by turning on the right FET's. Transistors Q570, Q580, Q583 and Q586 each turn on one FET, otherwise the -12.2 volts applied to their gate terminals turns them off. When the transistors are on, the FET's are on. Which transistors are turned on depends on the time per division selected from the front panel or by a remote program. That input is decoded internally to turn on the right transistors.

When FET Q575 is turned on by transistor Q570, there may be an unwanted shift in the output level to the comparator. That only happens when the zero decade (10^{-10}) is selected, giving a time/div of 500, 200 or 100 ps. To compensate for the shift, Q572 is also turned on and the current flowing through Q572 is

made adjustable with the 0 Decade Delay Zero pot R574. When Q572 is turned on (by Q570), its emitter goes close to ground level and zener diode D573 turns off. When not turned on, the base of Q572 goes to -12.2 volts and its emitter is clamped at -10 volts by the 10-volt zener diode.

The staircase amplitude at the input is 7.5 volts, having been divided down from 50 volts at the output of the staircase generator.

Besides the 0 to +7.5 volt staircase introduced to the operational amplifier, current is also introduced to the input from the output of another operational amplifier (Q360, Q370 and Q375 in the delay gating circuit) to offset the inverted staircase and provide "fine" delay for the CRT display. Offsetting the inverted staircase is the ordinary way to produce strobe delay. In most sampling scopes, the delay is called TIME POSITION and is controlled by a variable potentiometer. In the 3T5, the fine delay is controlled in increments of 0.1 ns for the zero (10^{-10}) decade (100 ps/div through 500 ps/div) and in increments of 1 ns for 1 ns/div through 1 µs/div range. The current introduced to offset the staircase is proportional to the delay produced thereby. The Delay Zero pot R391 permits the output level of the staircase inverting amplifier to be adjusted so the input to the comparator nearly matches the starting level of each fast ramp when zero delay is selected and zero offset current is applied. At 100 ps, 200 ps and 500 ps/div, the fastest fast ramp is nearly twice as long as the other fast ramps to accommodate three decades of fine (analog) delay. The other ramps accompany times scales that use no more than two decades of analog delay. Digitally counted, 100-ns clock cycles provide the longest initial (coarse) amounts of delay when all four decades of delay are used.


DIAL DELAY
PROGRAM SELECTOR
INT
EXT
J25
J24
+20V
16K
5.6K
20K
-12.2V
-100V
R327 10M
R329 90.9K
R335 8M
R338 4M
R337 2M
1M

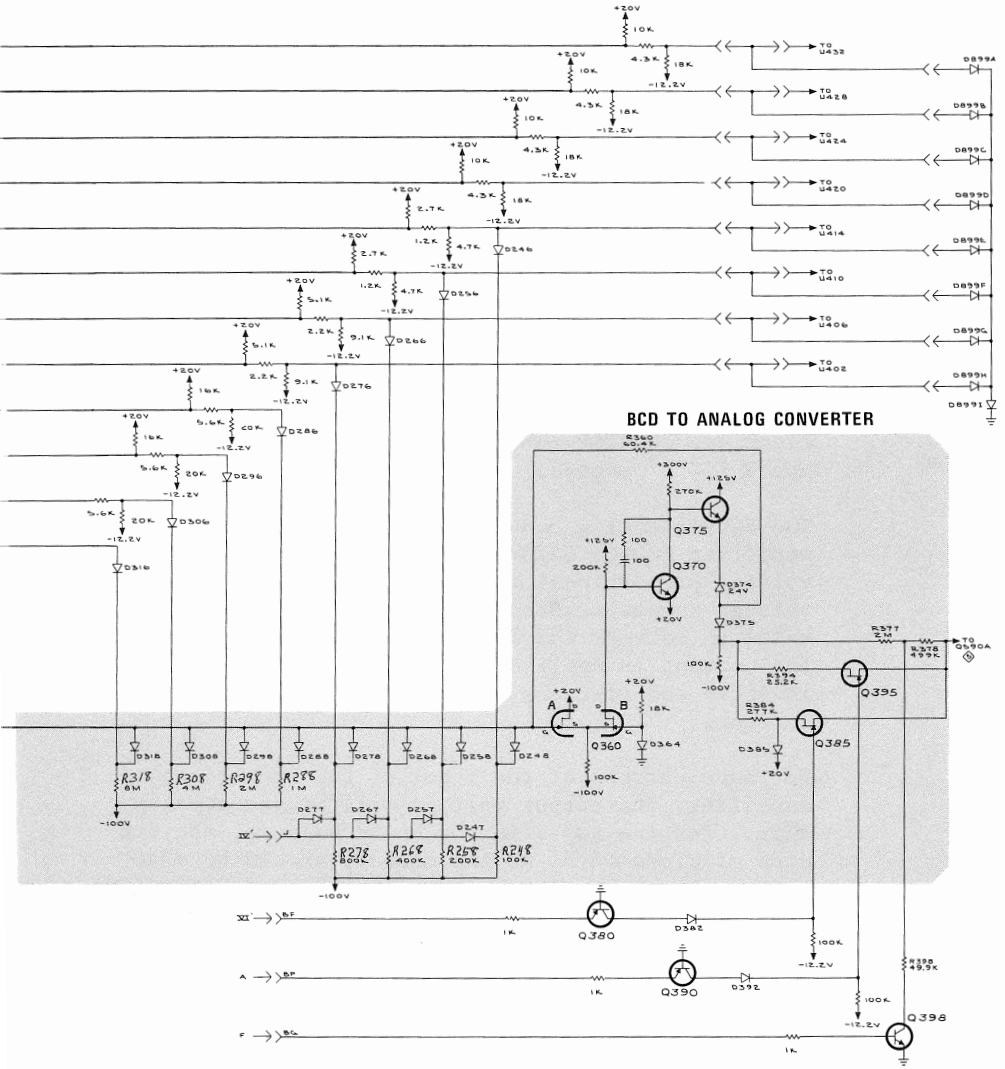


Fig. 5-6. 3T5 Delay Gating and Digital to Analog Converter.

3T5 DELAY-GATING AND DIGITAL-TO-ANALOG CONVERTER CIRCUITS

Four decades of time delay are selectable or programmable so the CRT may display the desired portions of a signal. The delay increments are either 0.1 ns, 1 ns or 100 ns, depending on the time/div selected. The 100-ns increments are produced by the gated 10-MHz clock. The 0.1 and 1-ns increments are produced by offsetting the inverted staircase by discrete amounts before applying it to the fast ramp comparator. The most significant delay decade (1000's) always employs the 10-MHz clock and a digital counter. The 100's delay decade also employs the clock and counter for all sweep ranges except the top speed (10^{-10} seconds) decade.

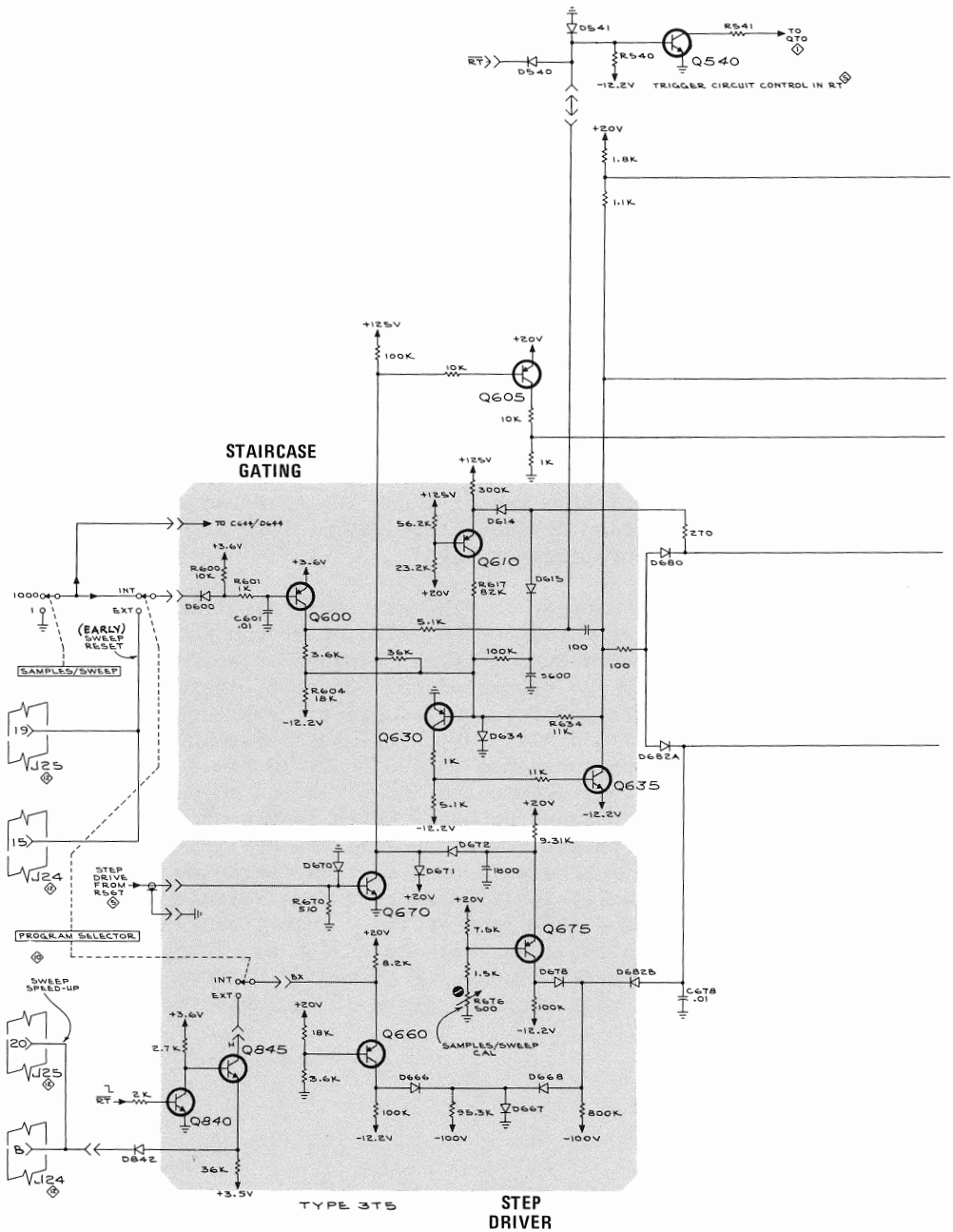
The BCD-to-analog converter is an operational amplifier (Q360, Q370 and Q375) that has an output voltage proportional to the input current. The output voltage drives a selectable resistor having a high value to convert the drive voltage to a drive current. The current is applied to the input of the staircase inverter and produces delay proportional to the current.

For zero current at the input of the operational amplifier, the output voltage will be practically zero. For the amplifier to be in balance, the top side of diode D375, at the output, should be +0.6 volts, the same voltage as at the gate of FET Q360B. Both FET Q385 and FET Q395 are off unless transistor Q380 or Q390 is turned on because both of the FET gate terminals are at -12.2 volts, enough to cut them

off. When Q398 is also off, the output resistance is 2.5 megohms, the series value of R377 and R378. Only one of the three transistors is turned on at any one time and sometimes none is on. The equivalent output impedance is controlled in four decade steps from 0.025 megohms to 25 megohms.

The input current to the operational amplifier depends on what combination of currents flowing through twelve resistors is diverted and applied to the input. The current for the least significant delay decade flows through R358, R348, R338 and R328. The bottom end of those resistors connects to a voltage divider comprised of R329 and R327 which sets the voltage at -10.

The current for the next most significant decade flows through R318, R308, R298 and R288. Ten times as much current flows through these resistors because they are connected to -100 volts instead of -10 volts. Current for the next decade flows through R279, R268, R258 and R248, which, because they have 1/10 the value of the previous decade, pass 10 times as much current as that decade and 100 times the current of the least significant decade. Which inputs are grounded determines which currents are applied to FET Q360A. The most significant of these three decades is normally inactivated by a plus voltage at the input to the line labeled IV'. This line is activated only when the time scale is at 100 ps, 200 ps or 500 ps/div. For other amounts of time/div, clocked delay is used for that decade instead of analog delay.


STAIRCASE GATING
STEP DRIVER
TYPE 3T5
TRIGGER CIRCUIT CONTROL IN RT
TO C644/D644
(EARLY) SWEEP RESET
SAMPLES/SWEEP
PROGRAM SELECTOR
STEP DRIVE FROM RS67
SWEEP SPEED-UP
SAMPLES/SWEEP CAL
INT
EXT
RT
Q540
Q605
Q610
Q600
Q630
Q635
Q670
Q675
Q660
Q845
Q840
D541
D540
D614
D615
D680
D682A
D682B
D634
D670
D671
D672
D678
D666
D668
D667
D642
+125V
+20V
+3.6V
-12.2V
-100V
+3.5V

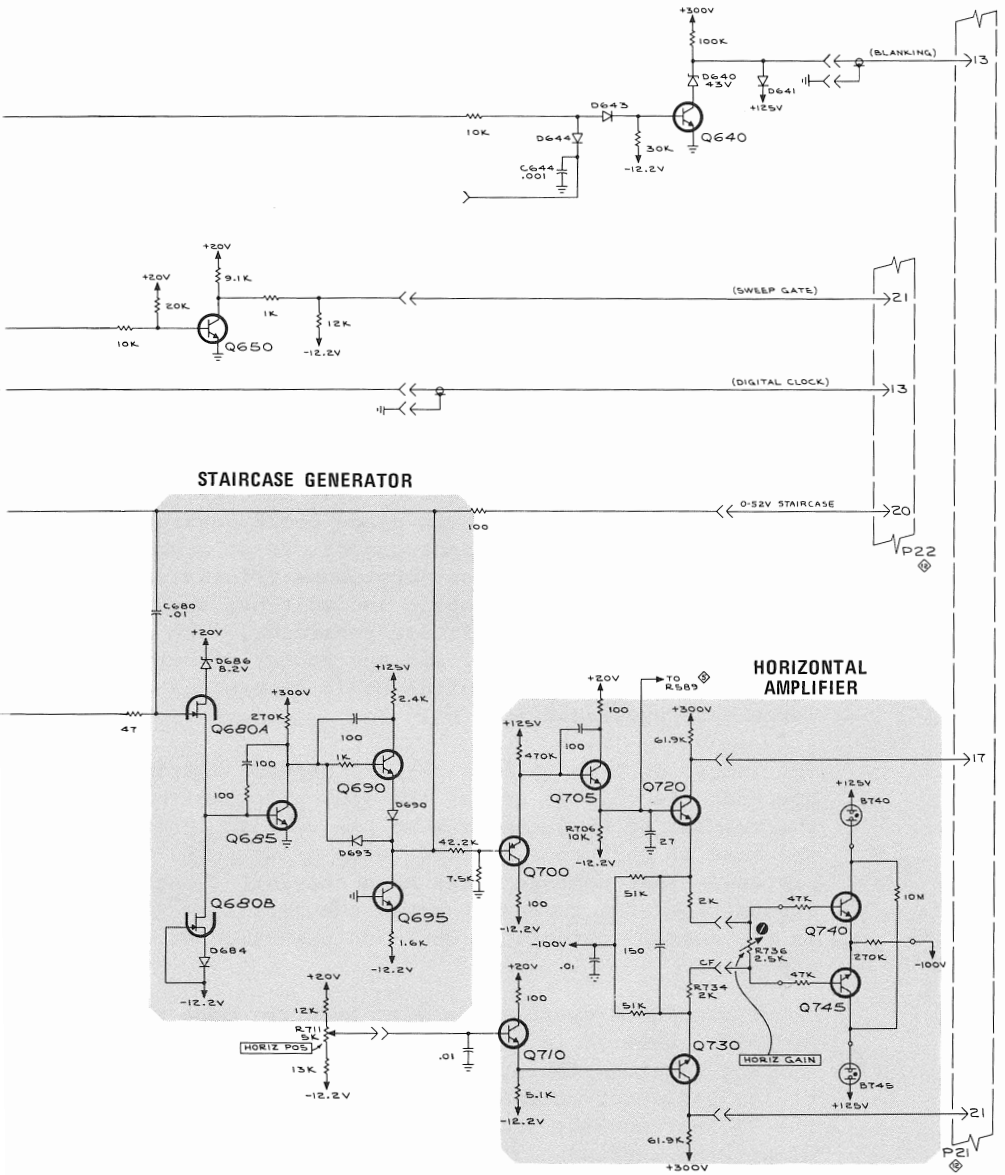


Fig. 5-7. 3T5 Staircase Gen and Horiz Amp.

3T5 STAIRCASE GEN AND HORIZ AMP CIRCUITS

STEP DRIVER

The step drive input transistor Q670 is normally off and the output driver transistor Q675 is normally on. Whenever a step drive pulse arrives at the input, it suddenly saturates transistor Q670 and diverts current from Q675, turning it off. Except when off, Q675 operates as an emitter follower with the emitter voltage determined by the Samples/Sweep Cal potentiometer R676 and the voltage divider resistors that are in series with it. When Q675 is conducting, most of the current flowing through it passes through diodes D678, D668 and D667. They clamp the collector voltage at about +1.5 volts which back biases diode D682B, the input diode to the staircase generator circuit. When Q675 cuts off, its collector voltage goes down and the current which flows through the 800-k resistor passes through diode D682B, charging the staircase generator input capacitors at a specific rate. That constant current continues briefly until transistor Q675 conducts again and switches the current away from the staircase generator. The amount of time Q675 is turned off and the amount of current which then flows through diode D682B determines how large each staircase step will be.

The length of time Q675 is cut off depends mostly on how soon the voltage across the 1800-pF capacitor at the emitter of Q675 can rise to the voltage level at the base of Q675 once an input step drive pulse expires. That voltage rises at a consistent rate, depending on the current through the 9.31-k resistor in the emitter circuit of Q675 and the value of the capacitor.

Transistor Q660 operates in very much the same way as Q675. When it is cut off by having its emitter current diverted through transistor Q845, that part of its collector current which was flowing through the 95.3-k resistor and diode D666 flows through diode D668 instead. That current adds to the amount contributed through the 800-k resistor and increases the size of the staircase steps by a factor of at least 10 to 1. When the INT-EXT switch is set to the internal position, transistor Q660 is always conducting and the size of the staircase steps should

always be right to produce a 1000-step sweep. When in the external position, where the 3T5 is controlled remotely instead of from the front panel, transistor Q660 may be on or off or alternately on and off, depending on the inputs to transistors Q840 and Q845. When the 3T5 is operating at 1 ms/div and slower, it is operating in the real-time mode and only a 1000-sample-sweep mode is permissible. In that case, the input voltage at the base of transistor Q840 turns it on, which turns off Q845 and leaves Q660 on. When the real-time mode is not programmed but the sweep speed-up feature is programmed, Q840 is left turned off and Q845 will be alternately on and off during a sweep. When the input voltage to diode D842 goes below the +3.5 volts level at the emitter of Q845, that transistor turns on and diverts current from Q660, which allows large stairsteps to be produced. Large stairsteps cause the sweeps to complete sooner. The time/div of the horizontal scale is not altered by this speed-up process as long as we don't try it with the real-time mode.

In the real-time mode, transistor Q840 is turned on and drives the base of Q845 close to ground, holding it off.

STAIRCASE GATING

When operated from the front panel using a 1000-sample sweep (100 dots per div), transistor Q600 is turned off and each staircase is started with a negative-going step-drive pulse at the collector of transistor Q670 in the step-driver circuit. Before a staircase is initiated, the staircase-gating multivibrator transistors Q630 and Q635 are both off because current through diode D634 back biases Q630. If set for a 1-sample "sweep," transistor Q600 is turned on and no step-drive pulse should cause the sweep-gating multivibrator to start the staircase generator. Likewise, when remotely programmed, a sweep may be prevented from starting anytime transistor Q600 is turned on, with a negative-step voltage at pin 19 of J25 or pin 15 of J24. Also, a negative step from one of these pins will switch the staircase-gating multi off anytime a staircase may be in progress. This should happen when the HIGH-SPEED feature is programmed.

The staircase is able to be stepped whenever diodes D680 and D682A are back biased. Those diodes become back biased when Q635 conducts and its collector voltage goes negative. After retrace and staircase holdoff, when a step-drive pulse arrives, it drives the collector of Q670 close to zero volts, reversing current through the 36-k resistor in its collector circuit and diverting current from diode D634 and forward biasing the base of transistor Q630. Both multivibrator transistors suddenly switch on and start a staircase.

As the staircase generator runs up, current increases proportionately through diode D615 and the 100-k resistor at its bottom end, diverting more and more current from the base of Q630. When the staircase voltage at the junction of diode D615 and D614 goes above the base voltage of transistor Q610 (+52 volts), the transistor conducts heavily and diverts the remaining current from the base of Q630, turning it off. That turns off Q635 and lets the staircase generator recover.

During the recovery period, the sweep-gating multivibrator is prevented from responding to new step-drive pulses for awhile by the extra current which flows through diode D634 and the 100-k resistor above it. The current is supplied by the charge stored in the 5600-pF capacitor at the junction of the 100-k resistor and diode D615 during the staircase run-up. After the staircase generator has recovered and enough charge has leaked off of the 5600-pF capacitor, transistor Q630 may again be turned on by a down-going step-drive pulse at the collector of Q670.

When a staircase goes high enough to cause transistor Q610 to conduct heavily and end the staircase, the retrace blanking transistor Q640 is turned on. Likewise, the sweep gate transistor Q650 is turned on. Both remain on until a new staircase is initiated.

Transistor Q540 is turned on momentarily at the end of each staircase sweep when the real-time mode is selected or programmed. It controls the trigger holdoff and counter-reset multivibrator in the trigger circuit when the real-time mode is selected.

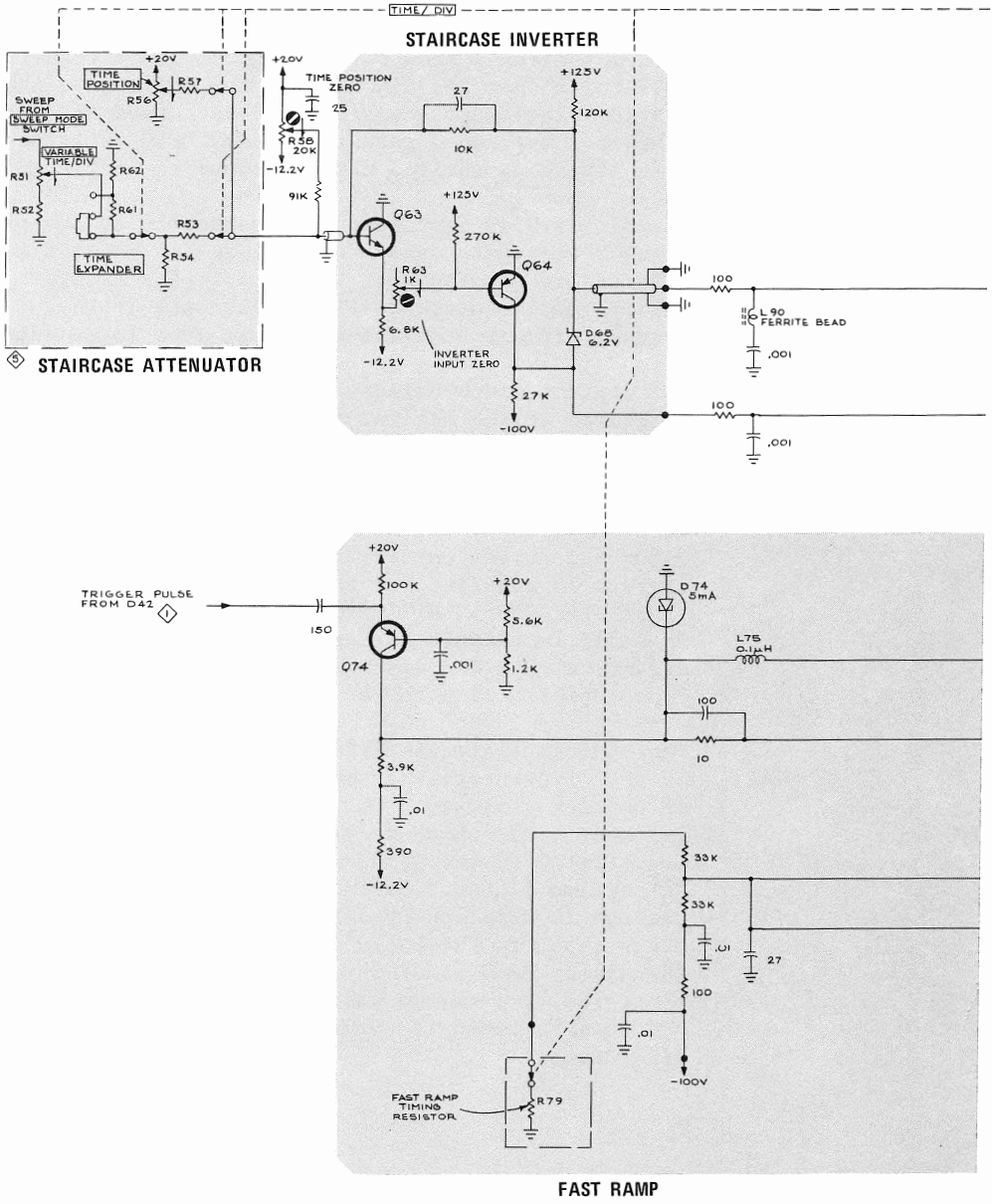
The digital clock pulses from transistor Q605 are delivered to the digital readout unit (Type 230 or 6R1A) for measuring time intervals.

STAIRCASE GENERATOR

High open-loop voltage gain is provided by transistor Q685. It is driven by source follower Q680A and drives emitter follower Q690. Constant current is supplied for the emitter follower by transistor Q695. Miller capacitor C680 is charged in small increments by current pulses from the step-driver circuit and discharges through disconnect diode D682A during retrace.

HORIZONTAL AMP

The 50-volt staircase is divided down to 15 volts by the 42.2-k resistor and 7.5-k resistor at the base of emitter follower Q700. Q700 drives emitter follower Q705, which drives one side of balanced amplifier Q720 and Q730, which drives the horizontal deflection plates. Horizontal trace positioning voltage is supplied by emitter follower Q710 to the other input to the balanced amplifier. Either transistor Q740 or Q745 turns on when the beam is not electrically centered horizontally, indicating where the beam is aimed if turned off or deflected off-screen.


TIME/DIV
STAIRCASE INVERTER
+20V
TIME POSITION
R57
R56
SWEEP FROM SWEEP MODE SWITCH
VARIABLE TIME/DIV
R51
R52
R62
R61
R53
R54
TIME EXPANDER
STAIRCASE ATTENUATOR
+20V
TIME POSITION ZERO
25
R58 20K
-12.2V
91K
27
10K
+125V
120K
+125V
270K
Q63
Q64
R63 1K
6.8K
-12.2V
INVERTER INPUT ZERO
27K
-100V
D68 6.2V
100
L90 FERRITE BEAD
.001
100
.001
TRIGGER PULSE FROM D42
150
+20V
100K
Q74
+20V
5.6K
.001
1.2K
D74 5mA
L75 0.1μH
100
10
3.9K
.01
390
-12.2V
33K
33K
.01
27
100
.01
-100V
FAST RAMP TIMING RESISTOR
R79
FAST RAMP

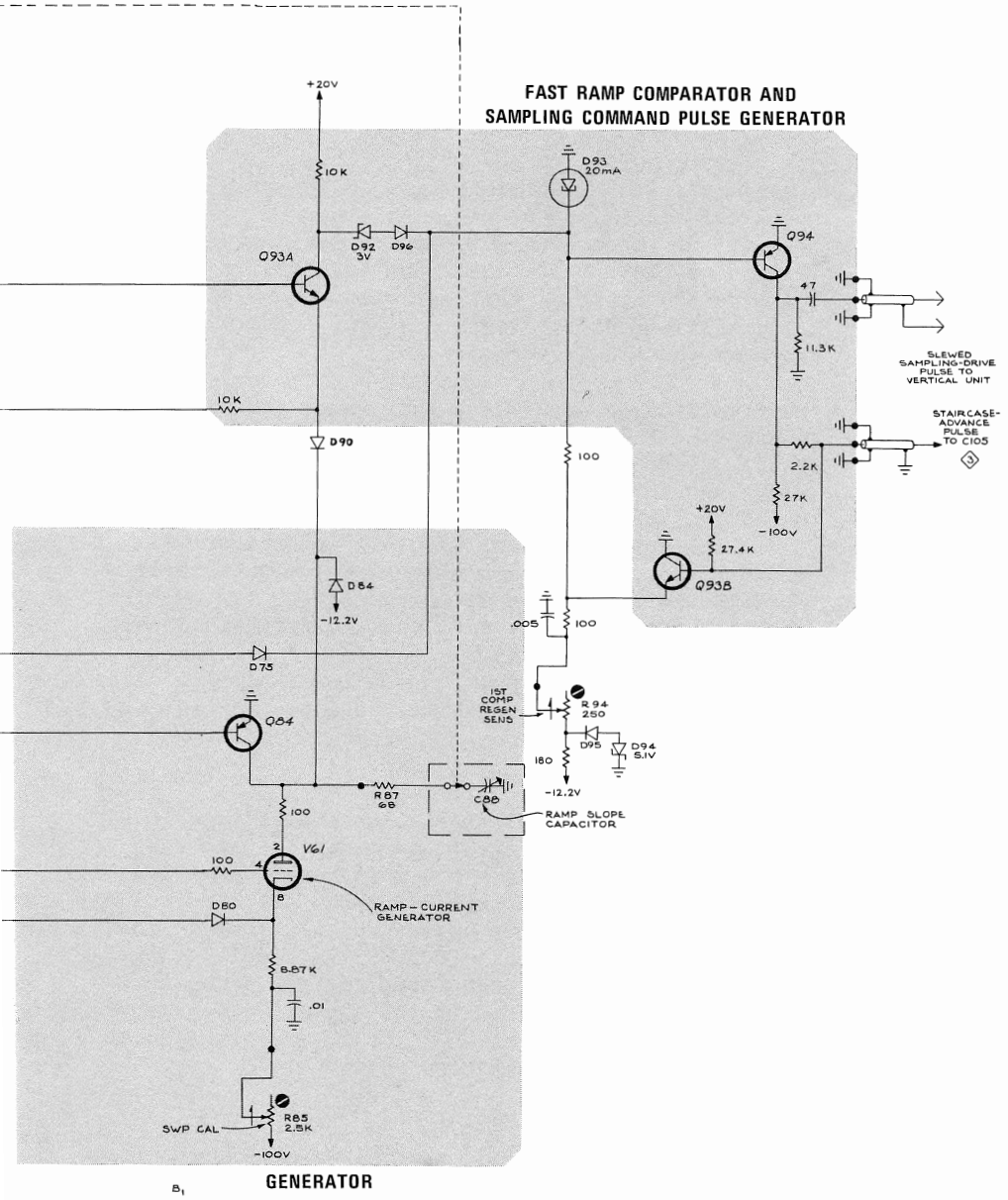


Fig. 5-8. 3T77A Fast Ramp.

3T77A FAST RAMP CIRCUITS

FAST RAMP GENERATOR

Vacuum tube V61 passes a constant current, the amount depending on its grid voltage and the total value of resistance in its cathode circuit. The grid voltage is normally close to -50 volts, determined by the values of the divider resistors in the grid circuit. Grid voltage is adjustable over a narrow range for two of the three time-position ranges where the ramp slope capacitor selected is not adjustable. That permits the slope of all fast ramps to be adjusted precisely. Variable resistors R79A and R79B are used to make those adjustments.

When waiting to generate a fast ramp, the plate current of V61 flows through transistor Q84 because tunnel diode D74 is switched to its higher voltage state and forward biases the base of Q84. About 3 mA normally flows through the tunnel diode and the 3.9-k collector resistor of Q74. Transistor Q74 conducts continually but only passes a very small current until a plus step is coupled to its emitter from the output tunnel diode in the trigger circuit. At that moment, Q74 diverts the 3 mA from tunnel diode D74 and switches it to its lower voltage state. That turns off Q84 and causes the plate current of V61 to flow through the ramp slope capacitor C88, producing a negative-going ramp.

A ramp runs down until it reaches the voltage level at the output of the staircase inverter. At that moment, comparison diode D90 conducts, lowers the voltage at the collector of Q93A and switches tunnel diode D93 (down) to its higher voltage state. The negative step at tunnel diode D93 is coupled back to tunnel diode D74, through diode D75 and inductor L75, and causes D74 to switch to its higher voltage state. That turns on transistor Q84, which ends that ramp and discharges the ramp capacitor.

In the 3T77A, each fast ramp ends and is reset at the moment it produces a sampling-command pulse.

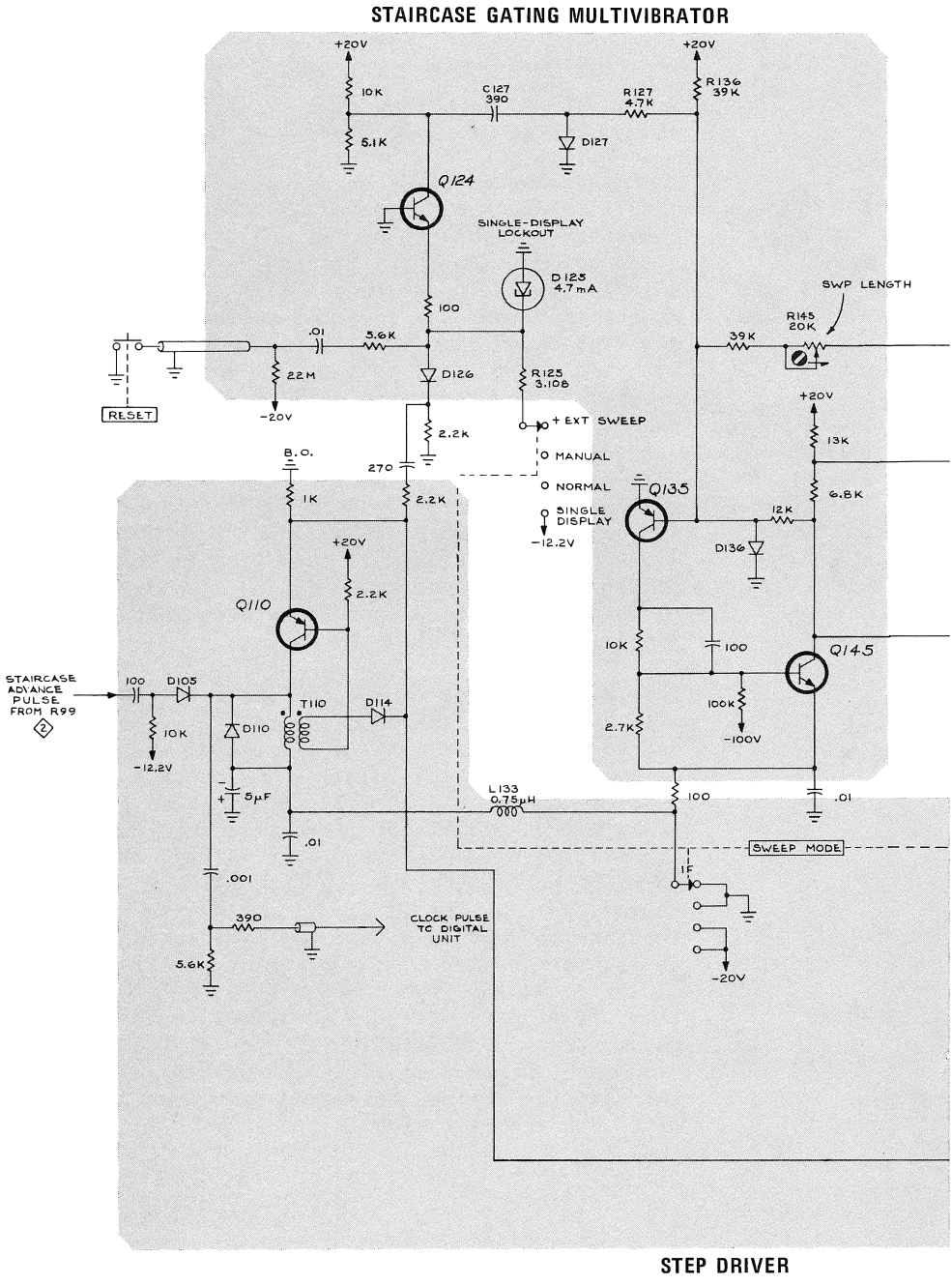
STAIRCASE INVERTER and STAIRCASE ATTENUATOR

The staircase inverter is an operational amplifier with a feedback resistor of 10 k and an input resistance, depending on the amount of staircase attenuation (time magnification) required. Adjustments of the circuit follow the same principles as the 1S1 staircase inverter adjustments. See the description of that circuit for more details (page 161).

FAST RAMP COMPARATOR and SAMPLING-COMMAND PULSE GENERATOR

Emitter follower comparator transistor Q93A normally passes a current of about 620 μA, determined by the 6.2-volt zener diode D68 in the staircase inverter circuit and the 10-k emitter resistance of Q93A. The collector voltage of Q93A is held at about +3.5 volts by the voltage drop across zener diode D92 and signal diode D96. A little more than 1 mA is normally diverted from tunnel diode D93 by the 10-k collector resistor and that current flows through the zener diode and diode D96.

The 1st Comp Regen Sens poteniometer R94 sets the bias current for tunnel diode D93. The pot must be set to pass a little bit more current than the peak point current of the tunnel diode so that when the current usually diverted by diode D96 is interrupted, it is enough additional current for the tunnel diode to make it switch to its higher voltage state. That turns on transistor Q94 and produces a sampling-command pulse. Before transistor Q94 is turned on, the base of Q93B is at about -7 volts, determined by the divider action of the resistors in the base circuit. Because the emitter of Q93B is higher than that, it is off until Q94 turns on. When Q94 turns on, it turns on Q93B, diverts current from tunnel diode D93, which then turns off Q94 and Q93B, ending the sampling-command pulse and resetting the tunnel diode for the next time.


STAIRCASE GATING MULTIVIBRATOR
+20V
10K
5.1K
C127
390
R127
4.7K
D127
R136
39K
Q124
SINGLE-DISPLAY
LOCKOUT
D125
4.7mA
100
.01
3.6K
22M
-20V
D126
R125
3.10B
RESET
+ EXT SWEEP
O MANUAL
O NORMAL
O SINGLE
DISPLAY
-12.2V
2.2K
270
B.O.
1K
2.2K
+20V
Q110
2.2K
SWP LENGTH
R145
20K
39K
+20V
13K
6.8K
Q135
12K
D136
10K
100
Q145
100K
-100V
2.7K
STAIRCASE
ADVANCE
PULSE
FROM R99
2
100
D105
10K
-12.2V
D110
T110
D114
5μF
L133
0.75μH
.01
.001
390
5.6K
CLOCK PULSE
TO DIGITAL
UNIT
100
.01
SWEEP MODE
1F
-20V
STEP DRIVER

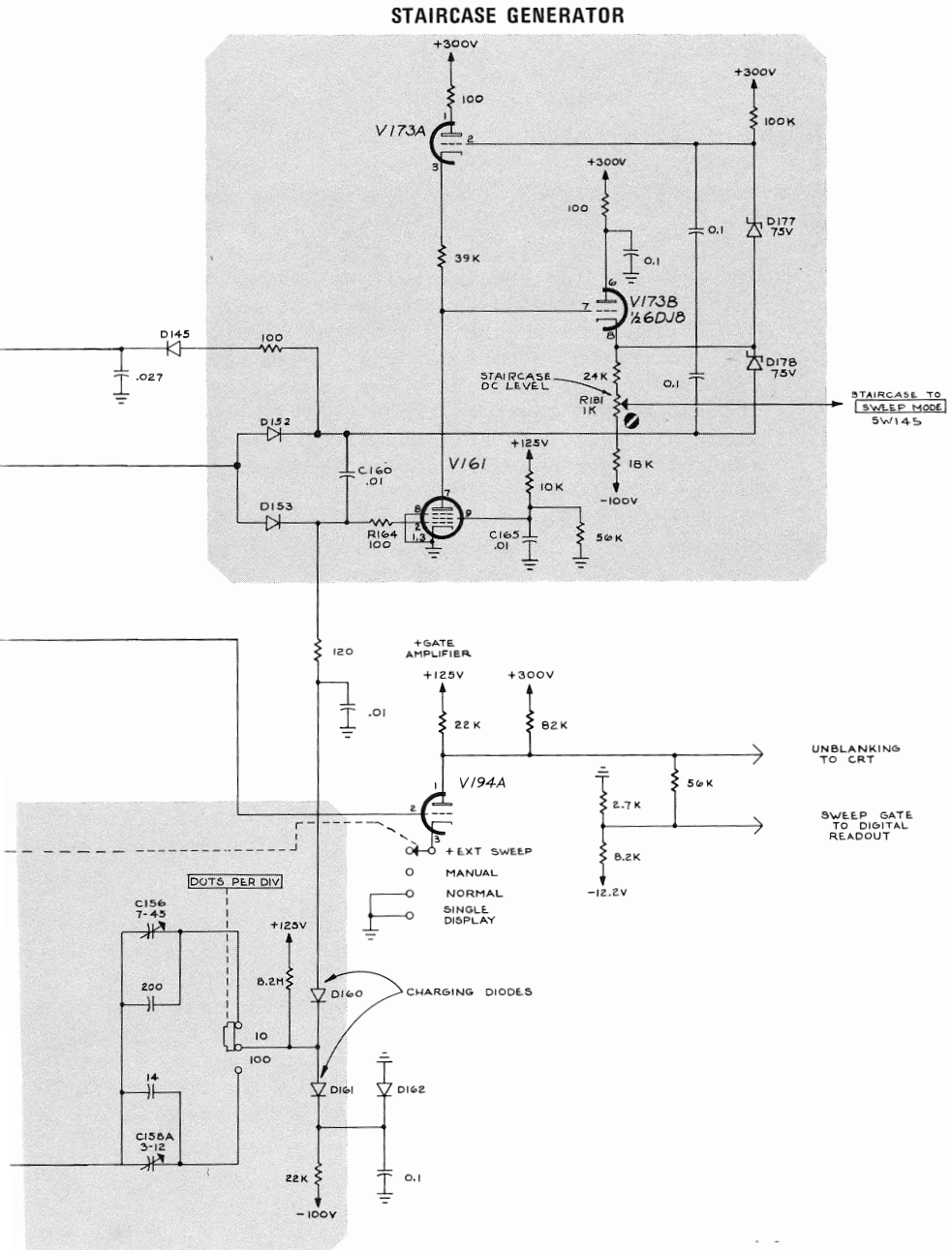


Fig. 5-9. 3T77A Staircase Generator.

3T77A STAIRCASE GENERATOR CIRCUITS

STEP DRIVER

Blocking oscillator transistor Q110 is normally off because its base-emitter junction is reversed biased by the forward voltage drop across diode D114. That current sets the emitter voltage between zero and +20 volts, depending on the ratio of the 1-k and 2.2-k resistors in series with the current. The emitter voltage determines the charge stored in capacitors C156 or C158A. When a positive step arrives at the input to diode D105, it is coupled through transformer T110 to the base of Q110, turning the transistor on. The action is regenerative and the transistor suddenly switches into saturation. Its emitter comes down and quickly drives the charge on capacitor C156 (or C158A) through diode D160 into the 0.01-μF capacitor that is located at the bottom end of the 120-ohm resistor. That charge transfers into the 0.01-μF Miller capacitor C160 in the staircase generator circuit and produces an output step. The emitter of Q110 also delivers a negative drive pulse to the emitter circuit of Q124 to start the staircase generator when necessary.

When the magnetic field in the blocking oscillator transformer collapses, transistor Q110 is cut off and diode D114 conducts again. Diode D110 passes current from the collapsing field.

STAIRCASE GATING MULTI-VIBRATOR

Transistors Q135 and Q145 comprise a bistable multivibrator. Both transistors are either on or off. Both are always off except in the NORMAL or SINGLE DISPLAY modes where -20 volts is connected to the emitter circuit of Q145 and the collector circuit of Q135. When waiting for a staircase gating pulse, both transistors are off. Diode D136 in the base circuit of Q135 is forward biased which keeps Q135 turned off.

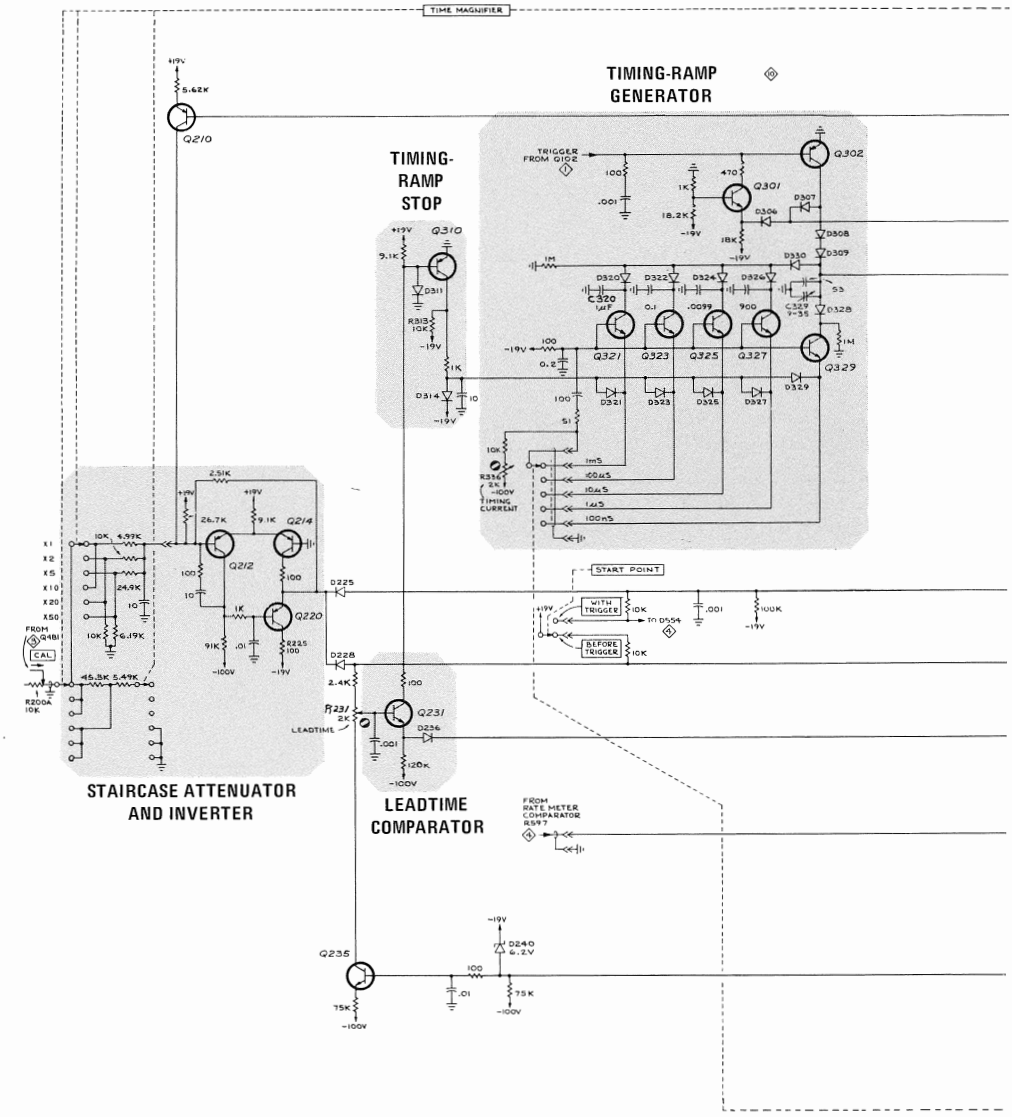
In the NORMAL mode, transistor Q124 is off until its emitter is driven negative by the step driver. That drives the collector of Q124 to ground and diode D127 below ground, momentarily diverting current from diode D136 and turning on Q135. When Q135 turns on, it turns on Q145 which holds Q135 on and starts the staircase generator.

Each step-drive pulse advances the staircase by the same amount. As the staircase runs up, diode D145 and Swp Length pot R145 pass more and more current, which diverts more and more base current from Q135. When the staircase reaches about +50 volts, depending on the setting of the Swp Length potentiometer, enough base current is diverted from Q135 to start to turn off Q145. Transistor Q145 then rapidly turns off Q135 and resets the staircase. The Miller capacitor then discharges. To give the capacitor time to completely discharge, drive pulses to the multivibrator transistors must be held off temporarily. The charge in the 0.027-μF capacitor near diode D145 serves that purpose by temporarily supplying enough additional forward bias current to diode D136 so that the drive pulses at the collector of Q124 can't turn on Q135.

In the SINGLE DISPLAY mode, tunnel diode D125 is connected to a source of bias current and passes about 3 mA. With that current it may be in either its lower voltage state or its higher voltage state, but the first pulse from the step driver switches it to its higher voltage state. It normally remains there and keeps Q124 saturated so that no drive pulses are coupled to the staircase gating multivibrator. However, when the RESET button is pressed, the tunnel diode switches to its lower voltage state and remains there until the step driver delivers its next pulse. At that time, the pulse is coupled to the gating multivibrator, turns on Q135 and starts a staircase.

6

RANDOM MODE CIRCUITS


TIME MAGNIFIER
TIMING-RAMP GENERATOR
TIMING-RAMP STOP
STAIRCASE ATTENUATOR AND INVERTER
LEADTIME COMPARATOR
Q210
Q310
Q302
Q301
Q321
Q323
Q325
Q327
Q329
Q212
Q214
Q220
Q231
Q235
START POINT
WITH TRIGGER
BEFORE TRIGGER
TRIGGER FROM GIDE
FROM RATE METER COMPARATOR R597
TIMING CURREAT
LEADTIME
CAL

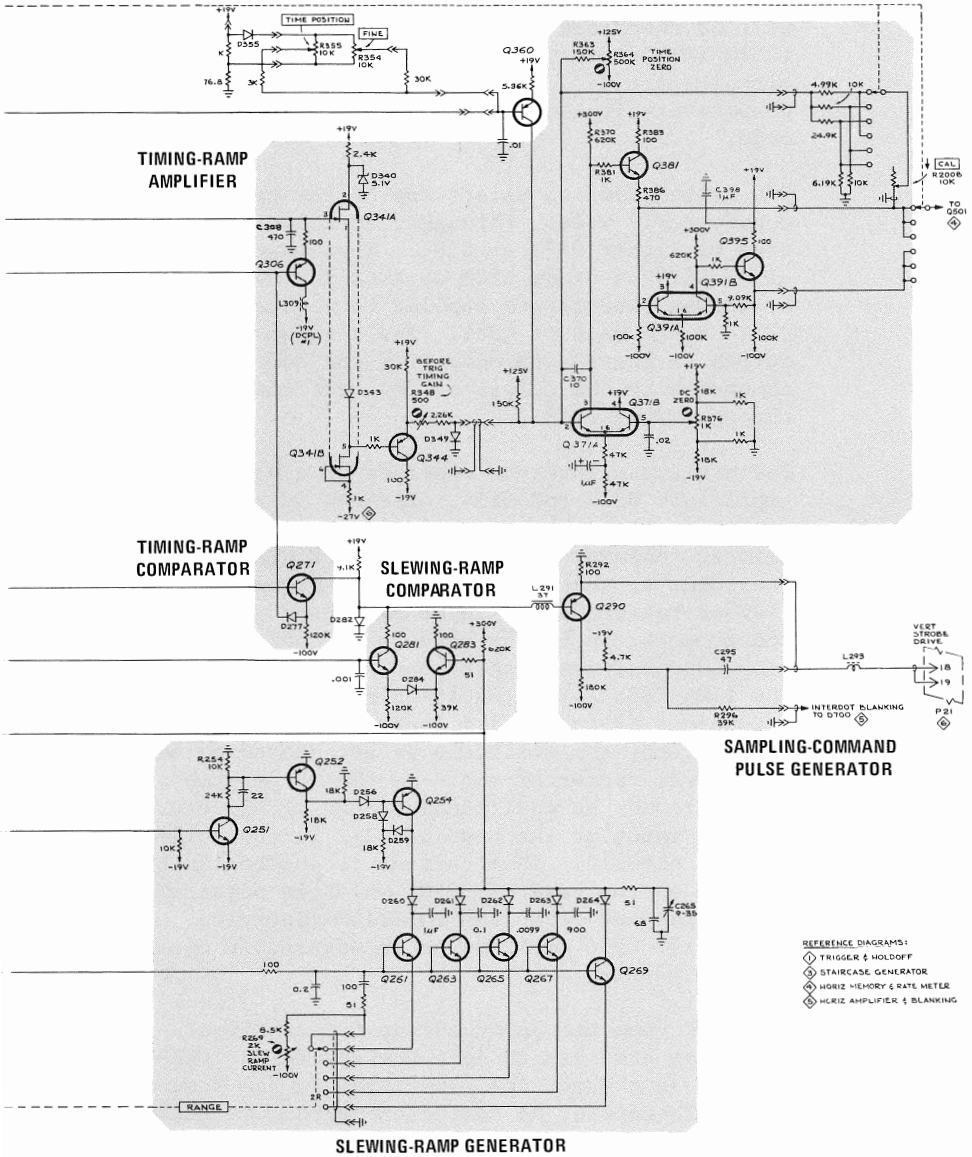


Fig. 6-1. 3T2 Ramp Generators.

3T2 RAMP GENERATORS CIRCUITS

Only the random (BEFORE TRIGGER) mode of operation will be described for the 3T2. In the sequential (WITH TRIGGER) mode, most of the ramp generator circuits are not operative. Only the timing ramp comparator circuit is not operative in the random mode.

The switch used to select one of the two modes connects +19 volts, through a 10-k resistor, to the base of either Q271 or Q281. That turns on either diode D225 or diode D228 so that the output of the staircase inverter is applied to either the base of Q271 or the base of Q281. The diagram shows the switch in the random mode with the base of Q281 connected to the output of the staircase inverter through diode D228.

STAIRCASE ATTENUATOR and INVERTER

The staircase inverter consists of a balanced amplifier, Q212 and Q214, operated as an operational amplifier with the output fed back to the input from emitter follower Q220 through the 2.51-k resistor. The input to the base of Q212 is through selectable divider resistors and input resistors that control the attenuation of the zero to +15 volt staircase from the staircase generator. In the X1 position of the TIME MAGNIFIER, the 15-volt staircase is attenuated by an initial factor of 2 to 1. In the X2 position, the staircase is attenuated by an additional factor of two. In the X5 position, it is attenuated by an additional factor of X5, etc. Another input at the base of Q212 is the collector current of Q210. That current is controlled by the voltage on the base of Q210, which is adjusted with the coarse and fine TIME POSITION controls. Transistor Q210 operates as an adjustable constant current supply.

Feedback from the balanced input operational amplifier attempts to hold the voltage at the base of Q212 at ground, the same level as the base of Q214. Therefore, as collector current increases in Q210, the output of the operational amplifier is offset further negative with respect to ground so that practically all of the current passes through the feedback resistor. The output may be offset from about zero (no delay) to about -7.5 volts (maximum delay) with the TIME POSITION controls.

The output is fed directly to one side of the slewing-ramp comparator through diode D228. The output is also fed (indirectly) to the base of transistor Q231, the leadtime comparator. A constant voltage drop exists between the output of the staircase inverter and the base of transistor Q231 because of the constant current passed by Q235 through the two resistors in series with its collector. The base voltage of Q231 is adjustable with the Leadtime offset pot R231. The pot is normally set so 6 divisions of baseline may be viewed ahead of the trigger-recognition point when using X1 TIME MAGNIFICATION and any TIME POSITION RANGE except 100 ns. In that range, it is typical to be able to display only about 1 division of baseline ahead of the trigger-recognition point when using X1 time magnification because a minimum of about 5 divisions (50 ns) is used to generate and deliver strobe pulses.

SLEWING RAMP GENERATOR

The first thing to happen in each new sampling cycle is that a plus pretrigger step is generated and arrives at the base of transistor Q251. That turns on Q252, which turns off Q254 and starts a slewing ramp running down from the collector of Q254. Before the pretrigger step arrived, the constant current flowing through Q261 also flowed through Q254. The base voltage of Q261 is close to -25.2 volts, determined by the 6.2-volt zener diode D240 connected to the -19 volt supply. That voltage is common also to the bases of Q263, Q265, Q267 and Q269. Only one of those transistors may conduct at any one time and which one it is depends on which one has its emitter connected by the TIME POSITION RANGE switch to the resistors that go to the -100 volt supply. A different ramp-slope capacitor is connected to each of the collectors of the five transistors. Which transistor is turned on determines which capacitor is selected and what the slewing ramp slope will be. The diodes in the collector circuits isolate the different capacitors. Only the diode in series with the selected transistor is turned on. Keep-alive current for that diode passes through the 620-k resistor that is connected to the 300-volt supply near the base of comparator transistor Q283.

When the plus step at the input to Q251 goes back down to -19 volts, Q251 turns off, which turns off Q252, which turns on Q254 and discharges the selected ramp slope capacitor. The constant current that charges the selected slewing-ramp capacitor is adjustable with the Slew Ramp Current pot R269 so that the slope of each slewing ramp may be the same as the slope of the corresponding timing ramp.

SLEWING RAMP COMPARATOR

Each slewing ramp is compared to a staircase level. Negative (inverted) staircase levels are applied to the base of Q281 and negative-going slewing ramps are applied to the base of Q283. Each slewing ramp starts above each staircase level and reaches that level on its way down. Transistors Q281 and Q283 act like separate emitter followers when the base of Q283 is higher than the base of Q281. As the base and emitter of Q283 follow down to the level of Q281, diode D284 conducts, turning on Q281 harder and turning on Q290. Transistor Q290 operates in an avalanche mode to produce a fast sampling-command pulse.

LEADTIME COMPARATOR

After a slewing ramp runs down and produces a sampling-command pulse, it continues until it reaches the lower offset level at the emitter of Q231. At that instant, diode D236 conducts and transistor Q231 turns on hard. A slewing ramp stops at that level because the emitter of Q231 is a low-impedance point.

TIMING RAMP STOP

When Q231 turns on hard, it turns Q310 on hard, which diverts all the emitter current from the constant current timing ramp transistor Q321. This, of course, stops the rundown of the timing ramp.

TIMING RAMP GENERATOR

As you may see, the timing ramp generator is very similar to the slewing ramp generator. Typically, timing ramps are initiated while a slewing ramp is running down. They are initiated by a positive step that occurs at the instant the input triggering signal is recognized by the trigger circuit. The step arrives at the base of Q302 and turns it off. The constant current passing through Q302, having no other path, charges the timing ramp slope capacitor C320 at a linear rate. When one of the five transistors other than Q321 is selected, a different timing capacitor is charged and the ramp slope changes accordingly. The capacitors are isolated by the diodes connected to the transistor collectors.

In the sequential mode, emitter follower Q271 is turned on all the time and is turned on hard the instant a timing ramp comes down slightly below the level of its emitter, generating a sampling-command pulse. In the random mode, each timing ramp is normally stopped on its way down when the ramp-stop transistor Q310 diverts current from the constant-current transistor that is selected. The stopped level must remain essentially constant until that level is amplified and gated into the horizontal memory. That moment is just prior to the moment when the ramps are reset. Emitter follower Q306 charges the relatively large 470-pF capacitor C308 to reduce the leakage rate of the fastest timing ramp capacitor while a stopped level is being amplified and gated into the horizontal memory. Emitter follower Q301 has an emitter level of about -1.5 volts. It holds the collector of Q302 far enough below ground so Q302 does not saturate and be slow to turn off. Diodes D306 and D307 connect the emitter of Q301 to the collector of Q302 except when Q302 is off and a ramp is running down. Diode D307 also provides a discharge path for the 470-pF capacitor C308. All the ramp generators are reset at the same time.

TIMING RAMP AMPLIFIER

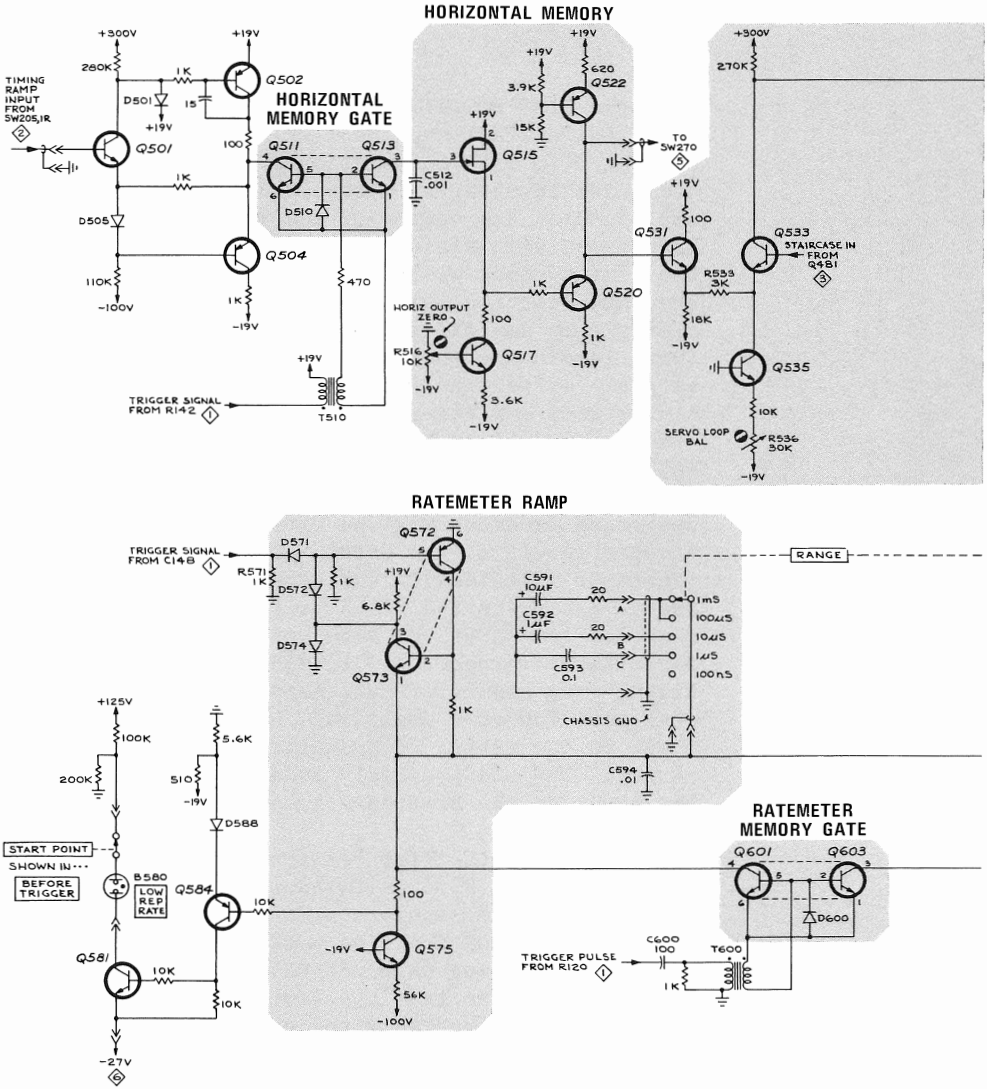
The timing ramp amplifier must provide a gain of from 2X to 100X to correspond to the 2X to 100X attenuation of the +15 volt staircase (X1 to X50 time magnification) so that the amplifier output may always cover the 15-volt range necessary to provide full-scale horizontal deflection. In other words, the output of the horizontal memory must be somewhere between 0 and +15 volts for the sample to be on-screen because the output of the timing ramp amplifier is gated into the horizontal memory without any further amplification, attenuation or offset. The same X1 to X50 time-magnifier switch controls the amplifier gain as controls the staircase attenuation. Ideally, the voltage range of stopped levels of a series of timing ramps will be the same as the amplitude of the associated staircase after the staircase is attenuated. However, any stopped levels outside of that range merely constitutes a wasted sample, one that would have to appear off-screen.

Field effect transistor Q341A is a source follower using Q341B as part of its source resistance to provide an approximate correction for temperature effects and a slight difference in gain at opposite extremes of input voltage. Because the current flowing through Q341A is the same current that flows through Q341B and because Q341B is operated at zero bias (gate shorted to source), Q341A also operates at practically zero bias. The drain of Q341B is therefore lower than the source of Q341A by the voltage drop across D343. The result is that the base of emitter follower Q344 is driven by a voltage one junction-drop lower than the gate of Q341A. And, because the emitter of emitter follower Q344 is one junction-drop higher than its base voltage, the emitter of Q344 is the same level as the source of Q341A.

Emitter follower Q344 drives the balanced, operational amplifier comprised of Q371A and Q371B that feeds back from emitter follower Q381 through selectable gain-setting resistors. The emitter follower also provides the amplifier output for the X1, X2 and X5 positions of the time magnifier. In the X10, X20 and X50 positions, the output is taken from emitter follower Q395. Transistor Q395 is part of a balanced 10X noninverting voltage amplifier with Q391. The 10X gain is primarily determined by the ratio of the 1-k resistor, at the base of Q391B, to the sum of its value and that of the 9.09-k divider resistor.

When the TIME POSITION controls are set for minimum delay (clockwise) and the TIME MAGNIFIER is set at X1, the 0 to +15 volt staircase at the input to the staircase inverter is attenuated 2X and has a 7.5-volt amplitude at the output of the inverter. Under ideal conditions with minimum delay, the stopped levels of the timing ramps will all be within a 7.5-volt bracket, starting near ground. The input to the timing ramp amplifier will, of course, be the same. Those levels are then amplified 2X, inverted, slightly offset and appear at the output of the timing ramp amplifier between 0 and +15 volts. Under similar conditions but with the TIME POSITION controls set fully counterclockwise (maximum delay), the 7.5-volt staircase amplitude at the output of the staircase inverter will be offset negative. The stopped levels at the output of the timing ramp generator will ideally correspond and be between about -8.0 volts and -15.5 volts. In order for that range of levels at the input of the timing ramp amplifier to produce a 0 to +15 volt output, the timing ramp amplifier must be offset, the same as the staircase inverter amplifier. Offset current at the input to the timing ramp amplifier is introduced through Q360 and precisely equals that supplied at the input to the staircase inverter through Q210.

The purpose of the Time Position Zero pot R364 and the DC Zero pot R376 is to assure that 0 to +15 volts at the output correctly tracks with the amount of amplification and the time position selected. The Before Trig Timing Gain pot R348 is to set the amplifier gain so that the time per division of the random mode is precisely the same as with the sequential mode.


HORIZONTAL MEMORY
HORIZONTAL MEMORY GATE
TIMING RAMP INPUT FROM SW205,1R
Q501
Q502
Q504
Q511
Q513
Q515
Q517
Q520
Q522
Q531
Q533
Q535
D501
D505
D510
C512 .001
HORIZ OUTPUT ZERO
R516 10K
TRIGGER SIGNAL FROM R142
T510
TO SW270
STAIRCASE IN FROM Q481
R533 3K
SERVO LOOP BAL
R536 50K
RATEMETER RAMP
TRIGGER SIGNAL FROM C148
Q571
Q572
Q573
D571
D572
D574
R571 1K
C591 10μF
C592 1μF
C593 0.1
C594 .01
RANGE
1mS
100μS
10μS
1μS
100nS
CHASSIS GND
RATEMETER MEMORY GATE
Q601
Q603
D600
C600 100
T600
TRIGGER PULSE FROM R120
START POINT SHOWN IN···
BEFORE TRIGGER
B580
LOW REP RATE
Q581
Q584
Q575
D588
+300V
+19V
+125V
-19V
-100V
-27V

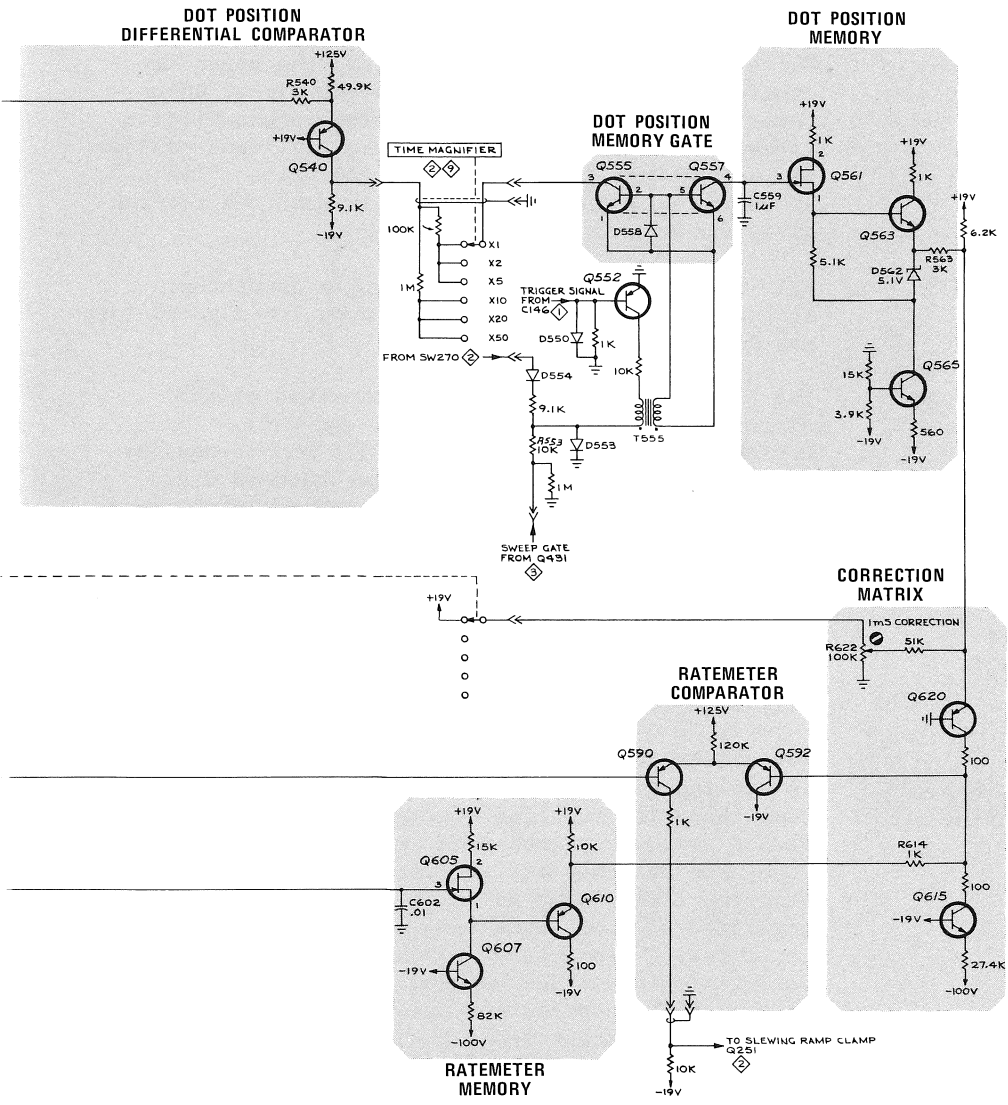


Fig. 6-2. 3T2 Horiz Memory and Rate Meter.

3T2 HORIZONTAL MEMORY AND RATEMETER CIRCUITS

The signal at the input to Q501, in the upper left-hand corner of the schematic, is the signal which comes from the output of the timing ramp amplifier circuit. Under normal conditions, the input voltage may be anywhere from 0 volts to +15 volts. That amount of voltage swing is what is required for ten divisions of horizontal deflection.

Only once each time a timing ramp is generated, stopped and amplified is the stopped level gated into the horizontal memory.

The horizontal memory gate is comprised of the circuits around transistors Q511 and Q513. The horizontal memory capacitor is C512 and it usually has a charge equal to some voltage between 0 and +15 volts. That capacitor must completely charge or discharge to the voltage level at the input to Q501 each time the memory gate conducts. And it must hold its charge for long periods; that is, have a slow leak-down rate. The drive for the memory capacitor must therefore be a low impedance when the memory gate conducts and the memory gate must be a very high impedance when not conducting.

HORIZONTAL MEMORY GATE

Transistors Q511 and Q513 only conduct when a pulse is applied through transformer T510. The rest of the time there is zero bias between base and emitter. Such pulses occur once each time a timing ramp is generated and they arrive just prior to the moment when the timing ramp is reset. Therefore, only amplified *stopped* levels are gated into the memory capacitor. When a pulse turns Q511 and Q513 on, any difference in voltage between the input and output of the gate causes current to flow through Q511 and Q513. When current flows in one direction, the collector-base junction of Q511 is forward biased and Q511 acts like a diode. When current flows in the other direction, the collector-base junction of Q513 is forward biased and it acts like a diode. Each time current flows, one transistor acts like a diode and the other acts like a transistor that is turned on hard. Diode D510 protects the base-emitter junctions of Q511 and Q513 from being excessively reversed biased when the field in transformer T510 collapses. Transistors Q501, Q502 and Q504 constitute a unity-gain noninverting low-impedance drive circuit

for the memory capacitor C512 for either charging or discharging the capacitor rapidly and completely. Q501 operates like an emitter follower driving another emitter follower Q504 for *discharging* the memory capacitor rapidly. In conjunction with Q502, it provides low-impedance drive for *charging* the memory capacitor completely and rapidly by virtue of the cascaded open-loop gain of Q501 and Q502.

HORIZONTAL MEMORY

The horizontal memory circuit provides a DC output equal to the voltage across the memory capacitor C512 without discharging the capacitor. The memory capacitor drives source follower Q515, which drives emitter follower Q520 that drives the output. Transistor Q522 is a constant-current supply for emitter follower Q520 and transistor Q517 is a constant-current supply for source follower Q515. The constant current passed by Q517 is adjustable with the Horizontal Output Zero control R516 to accommodate individual differences in the characteristics of FET Q515 so that the output voltage from the horizontal memory may be precisely the same as the voltage across the memory capacitor.

DOT-POSITION DIFFERENTIAL COMPARATOR

The dot-position differential comparator (amplifier) compares the output from the horizontal memory circuit with the existing step level at the output of the staircase generator and amplifies the difference. The staircase at the input to the base of Q533 runs from 0 to +15 volts. In the MANUAL SCAN mode, the input is also somewhere between 0 and +15 volts. The output from the horizontal memory is normally anywhere between 0 and +15 volts and, ideally, is at the same level as the existing step level from the staircase generator. The horizontal memory is charged (or discharged) once each time the staircase generator steps, so each new memory output is compared to a different step level. When the base of Q531 is the same level as the base of Q533, their emitters will also be at the same level and no current will flow through the 3-k resistor connected between emitters. When there is a difference in base levels, current will flow in one direction or the other, depending on which base level is higher. The current which flows through the resistor adds to the emitter current of either Q531 or Q533 and subtracts from the other. The difference in collector current through Q533 is therefore proportional to the difference in emitter levels.

Transistor Q540 is an emitter-coupled amplifier (through the 3-k resistor that comes from the collector of Q533) with its emitter slightly higher than the +19 volt level on its base. When the collector of Q533 goes up or down from +19 volts, it adds or subtracts from the emitter current of Q540 by an amount equal to the current through the 3-k resistor that goes between the collector of Q533 and the emitter of Q540. Because that resistor has the same value as the one between the emitters of Q531 and Q533, we can consider the current which flows through one flows through the other and a reversal of directions through one accompanies a reversal of direction through the other. Because the collector resistor of Q540 is about three times the value of its 3-k emitter resistor, Q540 provides a voltage gain of about 3X. Therefore, a one-volt difference between the output from the horizontal memory at a given moment and the staircase step level at that moment will show up at the collector of Q540 as about a 3-volt difference.

The collector of Q540 can swing between -19 volts and +19 volts, but is normally at zero volts when there is no difference between the base levels of Q531 and Q533. When the horizontal position of a dot is the same as it would be if the staircase was determining its position, there is no "dot-position difference" to amplify and Q540 collector should be close to ground potential. The Servo Loop Bal adjustment R536 helps assure this but is not normally adjusted to insure that condition. By observing where the horizontal dot position may be when using the MANUAL SCAN and WITH TRIGGER modes, the control is adjusted so the band of dots brackets that point when switching to the BEFORE TRIGGER mode.

DOT-POSITION MEMORY GATE

The gate at the input to the dot-position (difference) memory operates in the same way as the horizontal memory gate. See that discussion for details. One difference, however, is that the gate itself may be gated! Only when Q552 has a collector-supply voltage will a gating pulse at its base deliver a gating pulse to make Q555 and Q557 conduct. A negative collector-supply voltage is applied through R553 whenever a staircase is being generated. It is interrupted during the retrace interval. It is also interrupted all the time when the sequential mode is being used. A positive voltage is applied at

the top of diode D554 when in the sequential mode. That keeps the collector of Q552 close to ground potential by the divider action of the 9.1-k and 10-k resistors that are in series with diode D554.

DOT-POSITION MEMORY

Capacitor C559 is the memory capacitor, FET Q561 is a source follower which drives emitter follower Q563. Transistor Q565 is a constant-current supply for both the emitter follower and the source follower. The 5.1-volt zener diode D562 divides the available current so that a constant amount flows through the source follower. The memory capacitor is driven (when the gate conducts) from the collector of Q540 through either a 1-M resistor or a 100-k resistor, depending on the position of the TIME MAGNIFIER switch. Because the memory capacitor has a relatively high value and is charged or discharged through a relatively high resistance for only short intervals of time, the voltage across the capacitor is slow to change and requires a large number of gated inputs to change. The voltage across the capacitor, therefore, represents only a statistical average of a large number of dot-position difference errors. The emitter follower Q563 drives the emitter of Q620 through a 3-k resistor. We will come back to a discussion of Q620 and the error-correction matrix later.

RATEMETER RAMP

The ratemeter ramp generator consists of the circuits involving transistors Q572, Q573 and Q575 and ratemeter ramp slope capacitors C591, C592, C593 and C594. Transistor Q575 is a constant-current supply for the ramp-slope capacitor that has been selected by the (time position) RANGE switch. In the 100-ns range, capacitor C594 and the current through Q575 determines the slope of the ratemeter ramp. That ramp may have a duration of up to 100 μs, depending on the trigger-recognition rate. An interval of 100 μs is 1000 times longer than 100 ns. Each ratemeter ramp may last 1000 times the interval of the associated time position RANGE except for the longest, 1-ms range.

The ramps are negative going and run from a voltage close to ground down to about -19 volts before bottoming out. At -19 volts, the collector voltage of constant-current transistor Q575 is no higher than its base-voltage level so practically all the emitter current passes through the base lead.

Without an input trigger to the base of Q572 or with triggers that occur at too low a rate, the ratemeter ramp will bottom out at -19 volts.

Transistors Q572 and Q573 are normally both cut off because their bases have zero bias applied. Together they constitute a monostable multivibrator. When a negative signal arrives at the input to diode D571, it turns on Q572. The collector current turns on Q573 and its collector goes below ground, keeping the base of Q572 below the emitter. Both Q572 and Q573 conduct and discharge the ramp slope capacitor. When the collector of Q573 starts to go above ground, diode D572 disconnects and transistor Q572 turns off. Transistor Q573 turns off as soon as Q572 turns off because its base bias current is removed. Anytime a negative input signal arrives at diode D571 when the ramp is running down it will stop, reset and start running down again.

The ratemeter ramps are signaled to reset at the same instants when the slewing ramps and timing ramps are signaled to reset. It happens at the same rate as the input triggering signal is recognized. If the input triggering signal has a relatively low frequency and the intervals between cycles are therefore relatively long, the ratemeter ramps will have a high amplitude.

Anytime the triggering signal occurs at intervals greater than 1000 times the selected time-position range, the ramps will bottom out. When that happens, a neon light on the front panel (B580) should turn on. It comes on when Q581 is turned on by Q584. The emitter of Q584 is normally at about -18 volts and its base will not be lower than that except when the ratemeter ramps are about to bottom out.

RATEMETER MEMORY GATE

Q601 and Q603 are both off except when a pulse arrives at transformer T600. For details refer to the previous description of the horizontal memory gate.

RATEMETER MEMORY

The ratemeter (ramp amplitude) memory capacitor C602 is on the output side of the gate and is charged or discharged when the gate conducts. The ratemeter ramp slope capacitor charges or discharges the

ratemeter memory capacitor. The gate conducts for a short interval at the moments when the input triggering signal is recognized. This is always at least a little ahead of the moments when the ratemeter ramp is reset. The voltage stored in the memory capacitor is nearly equal to the amplitude of the ratemeter when the gate conducts.

The memory capacitor drives Q605, a source follower, which drives Q610, an emitter follower. Transistor Q607 provides a constant current for the source follower. The voltage at the output is essentially equal to the voltage on the memory capacitor and is normally between zero volts and about -18 volts, depending on the trigger-recognition rate and the capacitor selected.

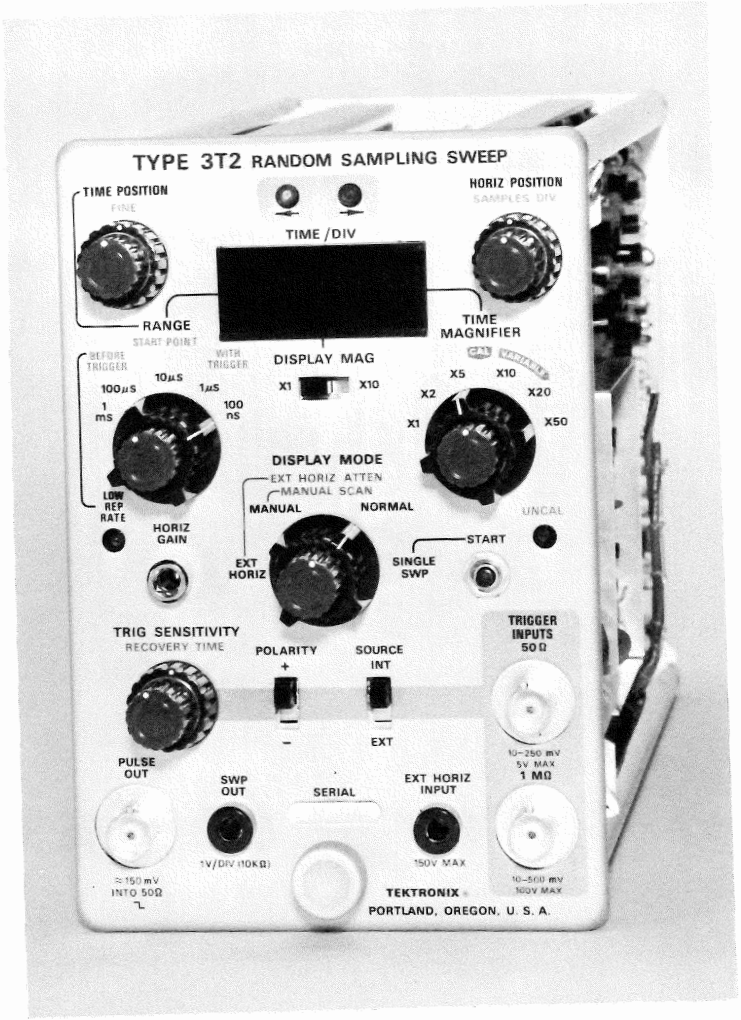
CORRECTION MATRIX

The current through transistor Q620 and the output voltage level of the ratemeter ramp memory jointly determine the voltage on the base of Q592. The voltage at that point determines how far the next ratemeter ramp must run down before generating a pulse to start the next slewing ramp. In other words, the voltage determines when the next pretrigger pulse will be generated. Transistor Q615 is a constant-current transistor and its current may all pass through Q620 or partly pass through the 1-k resistor R614. The voltage on the left side of the 1-k resistor is the principle voltage which determines the collector voltage of Q620 and Q615. Except for any voltage drop through the 1-k resistor, the emitter of Q610 sets the base level of Q592. The voltage at the base of Q592 is, therefore, equal to the voltage at the emitter of Q610 plus or minus the voltage drop through the resistor, depending on the direction of the current flow. Current through the resistor can be made to reverse by changing the emitter current of Q620 from less than the amount passing through Q615 to greater than that amount. Because the level at the base of Q592 must normally be a little higher than the bottom-peak amplitude of the ratemeter ramp, Q620 usually passes a little more current than passes through Q615. Q610 passes the rest through R614.

In the 1-ms range, where the same ratemeter ramp slope capacitor is used as in the 100-μs range, the base level of comparator transistor Q592 is offset slightly positive. With the 1-ms Correction pot R622, it is possible to compensate for the relatively steeper slope of the ramp capacitor and help the servo loop reach a stable statistically average rate voltage sooner.

RATEMETER COMPARATOR

Most of the time the base of Q590 is higher than the base of Q592, so Q590 is cut off most of the time. When cut off, the collector of Q590 is at -19 volts. When the base of Q590 comes down to the level of the base of Q592, current switches from Q592 to Q590 and a positive step at the collector of Q590 starts the slewing ramp.


TYPE 3T2 RANDOM SAMPLING SWEEP
TIME POSITION
FINE
TIME /DIV
HORIZ POSITION
SAMPLES DIV
RANGE
START POINT
TIME MAGNIFIER
BEFORE TRIGGER
WITH TRIGGER
DISPLAY MAG
100µS
10µS
1µS
1 ms
100 ns
X1
X10
X5
X2
X20
X50
DISPLAY MODE
EXT HORIZ ATTEN
MANUAL SCAN
MANUAL
NORMAL
LOW REP RATE
HORIZ GAIN
EXT HORIZ
SINGLE SWP
START
UNCAL
TRIG SENSITIVITY
RECOVERY TIME
POLARITY
SOURCE
INT
EXT
TRIGGER INPUTS 50Ω
10–250 mV 5V MAX
1 MΩ
PULSE OUT
≈150 mV INTO 50Ω
SWP OUT
1V/DIV (10KΩ)
SERIAL
EXT HORIZ INPUT
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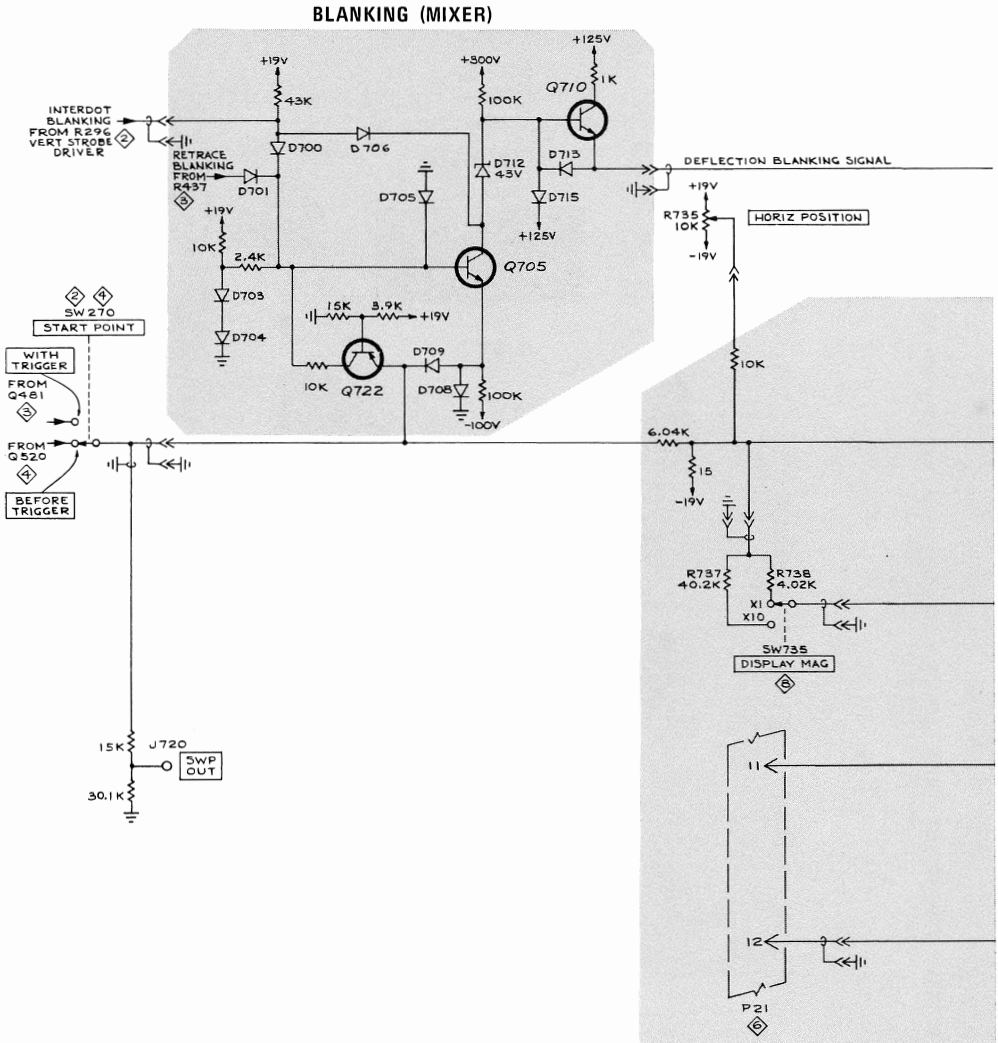
10–500 mV 100V MAX
TEKTRONIX
PORTLAND, OREGON, U. S. A.


BLANKING (MIXER)
+19V
43K
+300V
100K
+125V
1K
Q710
INTERDOT BLANKING FROM R296 VERT STROBE DRIVER
2
RETRACE BLANKING FROM R437
3
D700
D706
D701
D705
D712 43V
D713
D715
DEFLECTION BLANKING SIGNAL
+19V
R735 10K
HORIZ POSITION
-19V
+125V
10K
2.4K
Q705
D703
D704
15K
3.9K
+19V
10K
Q722
D709
D708
100K
-100V
2 4
SW270
START POINT
WITH TRIGGER
FROM Q481
3
FROM Q520
4
BEFORE TRIGGER
10K
6.04K
15
-19V
R737 40.2K
R738 4.02K
X1
X10
SW735
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30.1K
11
12
P21
6

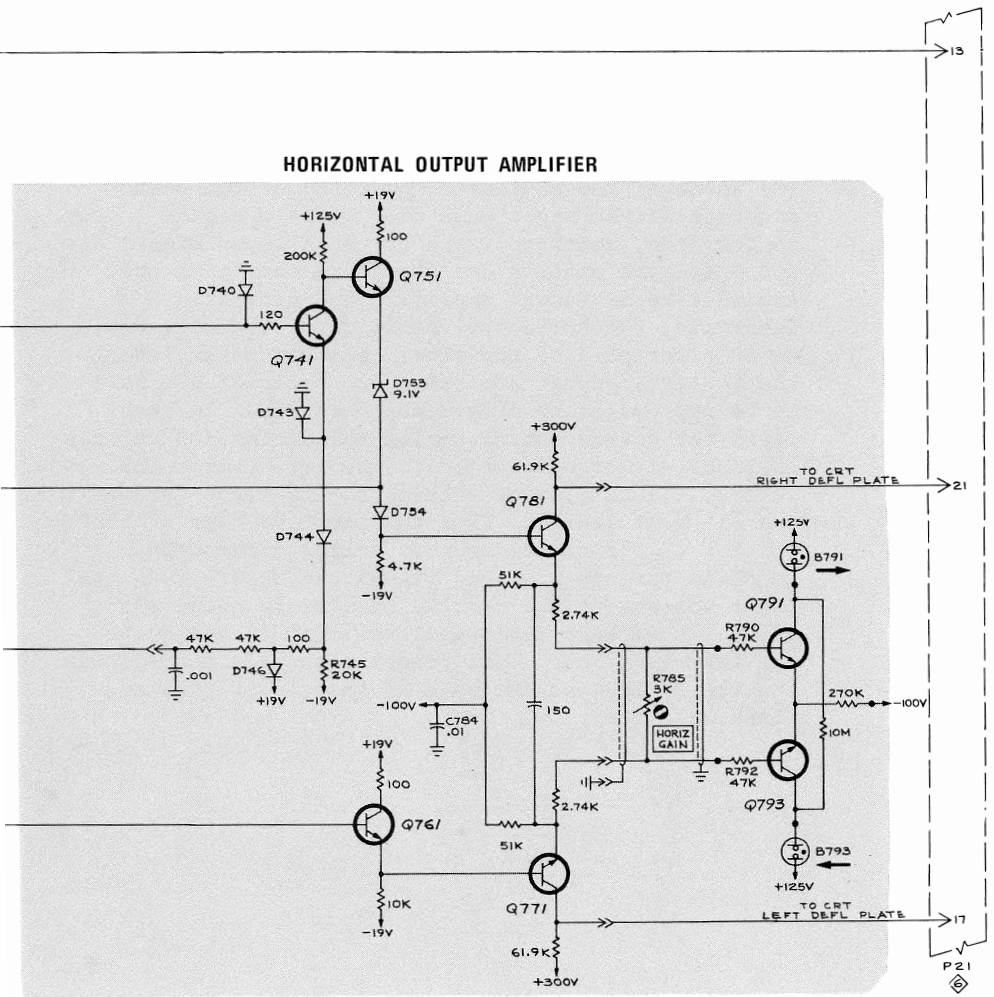

Fig. 6-3. 3T2 Horiz Amplifier and Blanking.

3T2 HORIZ AMPLIFIER AND BLANKING CIRCUITS

BLANKING MIXER

The blanking mixer blanks the CRT beam (1) during retrace intervals, (2) when a new sample is being amplified, stored and waiting to be displayed, and (3) whenever the horizontal position of the beam might be off-screen. When the 3T2 is operated in the random mode, samples of the vertical input signal are not displayed until a corresponding sample of the timing ramp is taken, amplified and stored. Otherwise, the horizontal position of the dots would be in error part of the time. Sometimes samples of the vertical signal are taken too early or too late to be appropriately displayed on-screen. In that case, the corresponding horizontal deflection voltage would be either off-screen to the left (below the zero-volt level) or off-screen to the right (above the +15 volt level). When the input voltage at the emitter of Q722 is below zero volts, diode D709 conducts through Q705 and blanks the beam. When the input voltage at the emitter of Q722 is above +15 volts, it exceeds the base level of Q722 and turns the transistor on. That raises the collector voltage and the voltage at the base of transistor Q705 and blanks the beam.

The base voltage of Q705 may also be elevated to blank the beam by a retrace blanking pulse at diode D701 or by an interdot blanking pulse at diode D700.

When Q705 turns on, it saturates. The output blanking pulse is coupled through diode D713 and comes down from +125 volts to +43 volts, the voltage drop across zener diode D712. Emitter follower Q710 is used to drive the stray capacitance of the deflection-blanking circuits for quick turn on after blanking.

HORIZONTAL OUTPUT AMPLIFIER

Transistors Q741 and Q751 are an operational amplifier with gain determined by the ratio of the feedback resistor (4.02-k or 40.2-k) and the 6.04-k input resistor. The 9.1-volt zener diode D753 sets the collector voltage of Q741 at about +9 volts for a zero-volt input and output signal. Emitter follower Q751 drives one input to the balanced deflection amplifier. The gain of the amplifier is set with the HORIZ GAIN pot R785 to match the deflection sensitivity of the CRT and set the time per division correctly. Whenever the beam is not near horizontal center, a considerable voltage will exist across R785, the HORIZ GAIN pot. That turns on one of the beam-position-indicator bulbs, indicating where the beam is aimed, if extinguished or off-screen.

7

DEFINITIONS OF TERMS

balanced sampling gate - A type of *sampling gate* arranged so that *strobe* currents are balanced to minimize kickout.

baseline drift - Vertical movement of the entire trace under constant signal conditions and control settings.

baseline shift - Vertical movement of the entire trace initiated by a change-of-signal conditions or control settings; usually reaches an equilibrium state more rapidly than *baseline drift*.

bridge, sampling - See *balanced sampling gate*.

blowby - A display aberration resulting from signal-induced displacement current through all capacitance shunting the *sampling gate*. Character of the aberration depends on the circuit time constants affecting redistribution of the displacement charge. See Fig. 7-1.

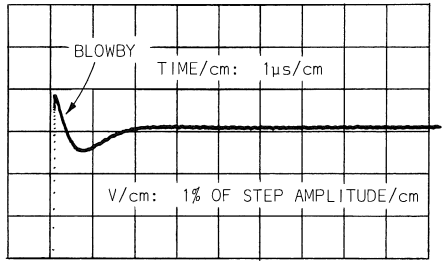

Fig. 7-1.

coherent display - A display in which the time-sequence of signal events is preserved. A coherent display may be produced by either *random* or *sequential sampling*.

countdown - In a circuit receiving a recurrent triggering signal, the process of responding to only every n^{th} recurrence of the signal where "n" is an integer which may or may not be constant.

display magnifier (horizontal) - A control or circuit whose function is to decrease the sweep-time per division of a display by increased gain in the horizontal amplification system.

display window - The particular time interval represented within the horizontal limits of the graticule. See *time window*.

dot - A displayed spot indicating the horizontal and vertical coordinates of a particular sample.

dot density - The number of dots per horizontal division.

dot response - See *dot transient response*.

dot slash - Dot elongation due to *memory* or *staircase* leakage.

dot transient response - The ability of a *sampling oscilloscope* to display correctly voltage change between any two successive samples. Good dot transient response requires unity *loop gain*.

dynamic range - In a system or instrument, the ratio of the specified maximum input-signal capability to the noise value.

equivalent time - The time scale represented in the display of a sampling oscilloscope operating in the *equivalent-time sampling* mode.

equivalent-time sampling - A sampling process in which at least one repetitive signal event is required for each sample taken. The time required for display construction is thus greater than the time represented in the display.

false display - A sampling display allowing faulty or ambiguous interpretation, usually caused by insufficient *dot density* or improper triggering.

fast ramp - See *slewing ramp*.

feedback attenuation - In a *sampling loop*, the effective intersample attenuation in the signal path between *memory* output and input *sampling gate*.

feedback attenuator - A circuit causing *feedback attenuation*. In a *sampling oscilloscope*, the control (mV/div) which determines vertical deflection factor and with the *forward attenuator* maintains constant *loop gain*.

feedback loop - See *sampling loop*.

forward attenuator - A circuit which determines *forward gain*, normally ganged with the *feedback attenuator*.

forward gain - In a *sampling loop*, the effective gain between the input *sampling gate* output and *memory* output.

kickout - A signal emanating from an input connector. See *trigger kickout* and *strobe kickout*.

lead time - The maximum time interval which may be displayed prior to the *trigger-recognition point*.

loop gain - In a *sampling loop*, the product of *sampling efficiency*, *forward gain* and *feedback attenuation*. Loop gain is normally unity except in a *smoothed display* where it is less than unity.

magnifier - See *display magnifier* and *time magnifier*.

memory - A circuit which stores the vertical (or horizontal) coordinate value of sample.

memory gate - An electronic switch between a *memory* and its driving amplifier.

memory slash - See *dot slash*.

offset monitor - A terminal that provides an output voltage proportional to the internal *DC offset voltage*.

pretrigger - A trigger signal which occurs before a related signal event.

random sampling - A sampling process involving significant time-interval uncertainty between the signal and the sample-taking operation. Also the process of *coherent display* construction from such randomly-taken samples. May be employed by either *real-time* or *equivalent-time sampling* oscilloscopes.

random sampling oscilloscope - An oscilloscope employing the *random sampling* process together with means for constructing a *coherent display* from the randomly-taken samples.

real time - The time scale associated with signal events.

real-time sampling - A sampling process in which more than one sample is taken for each signal event. The time required for display construction is the same as the time represented in the display.

reflection coefficient (ρ, rho) - In *time-domain reflectometry*, the ratio of peak amplitude of a particular reflection to the incident-step amplitude. In practice, the observed reflection coefficient may depend upon system risetime, losses in the associated transmission medium and the nature of reflection-producing discontinuity.

sampling density (Samples/Div) - See *dot density*.

sample distribution - In a *random sampling* oscilloscope, a function (mathematical) of *equivalent time* which describes how the density of randomly-placed samples varies across the signal.

sampling - A process of sensing and storing one or more instantaneous values of a signal for further processing or display.

sampling bridge - See *balanced sampling gate*.

sampling command - A trigger or other electrical signal intended to initiate or cause *sampling*. See *strobe*.

sampling efficiency (E) - The ratio of the voltage change between the instant before sampling t^- and the instant after sampling t^+ at the output of a *sampling gate* to the difference between gate input voltage, E_i, and gate output voltage, E_o, at the instant before sampling.

$$E = \frac{E_o(t^+) - E_o(t^-)}{E_i(t^-) - E_o(t^-)}$$

sampling gate - An electronic switch which conducts briefly upon command for the purpose of collecting and storing the instantaneous value of a signal.

sampling loop - Those circuits providing the main signal path through the input *sampling gate*, amplifiers, *forward gain* attenuator, *memory gate*, *memory*, *feedback attenuator* and back to the *sampling gate*.

sampling oscilloscope - An oscilloscope which employs *sampling* together with means for constructing a *coherent display* of the samples taken.

scanning - The process by which *slewing* is controlled. In an equivalent-time sampling oscilloscope, usually governed by a relatively slow *staircase* or ramp, manual control, or externally-derived signal.

sequential sampling - A *sampling* process in which samples are taken at successively later times relative to the *trigger-recognition* point.

slewing - The process of causing successive samples to be taken at different instants relative to the *trigger-recognition point*. See, also, *random sampling* and *sequential sampling*.

slewing ramp - A linear ramp which acts with a slower staircase, ramp, or other changing voltage to cause slewing.

slideback - A measurement process by which the value of a known is varied and compared with an unknown until they are equal (null).

smoothed display - A display produced by a *sampling loop* employing *smoothing*.

smoothing - A process affecting *dot transient response* intended to reduce the effect of random noise or jitter in the display.

strobe - A pulse of short duration which directly operates the *sampling gate* (See *sampling command*).

strobe kickout - A *strobe* signal emanating from the input connector.

tangentially-measured noise (tangential noise) - A noise value determined by a *tangential-noise measurement*.

tangential-noise measurement - A procedure to determine displayed noise wherein a flat-top pulse or squarewave input signal is adjusted in amplitude until the two traces (or portions of two traces) thus produced appear to be immediately adjacent or contiguous. Measurement of the resulting signal amplitude determines a noise value which correlates closely with the value interpreted by the eye from a sampling display and is called the "tangential noise value." See waveforms in Fig. 7-2.

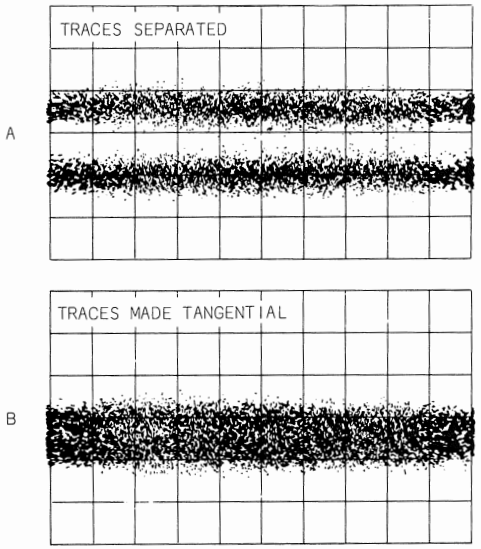

Fig. 7-2.

time domain reflectometry - The technique of launching a pulse or step signal into a transmission medium with subsequent analysis of any reflections thus produced.

time expander - See *time magnifier*.

time magnifier - A control which acts to alter the *equivalent-time* scale without an accompanying change in *dot density*. May magnify about a fixed point in the display. See also *display magnifier*.

time position - The *equivalent-time* relationship between the start of the *time window* and the *trigger-recognition point*. Also a control to vary this relationship.

time-position range - The *equivalent-time* interval over which the start of the *time window* may be positioned by the *time-position* control. The time position range normally starts before the *trigger-recognition point* in a *random-sampling* oscilloscope and with (or shortly after) the trigger-recognition point in a *sequential-sampling* oscilloscope (assuming no signal delay lines).

time window - The particular *equivalent-time* interval over which signal events can be described by *usable samples*. May be greater than the *display window*.

trigger kickout - A signal emanating from a trigger input connector or circuit.

trigger pickoff (trigger takeoff) - A device or circuit intended to extract a portion of the input signal for purposes of triggering the display.

trigger recognition - The process of responding to a suitable triggering signal.

trigger-recognition point - The points in time at which *trigger recognition* occurs, also that point on a displayed waveform representing the instant of *trigger recognition*.

twosie display - A *false display* formed by taking samples alternately along a pulse and its baseline, which can be a useful indication of *loop gain*. See Fig. 7-3.

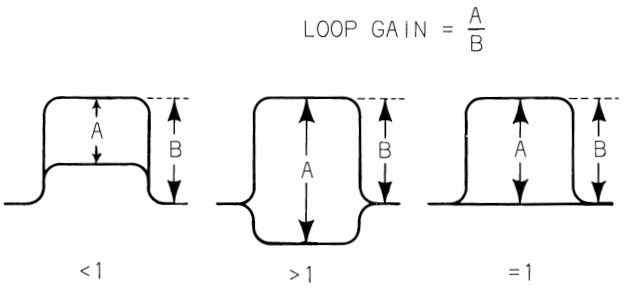

Fig. 7-3.

usable samples - Those samples containing signal information which is within the operating range of the *sampling loop*.

window - See *time window* and *display window*.

SUBJECT INDEX

(Also see definitions of terms, p227)

INSTRUMENT DIAGRAM INDEX

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INDEX TO CIRCUIT DESCRIPTIONS: SAMPLING, AMPLIFYING, and HOLDING CIRCUITS

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Sampling Command Pulse Regenerator	——	——	——	——
Gating Pulse Generator	——	——	——	——
Blocking Oscillator Driver	——	——	——	——
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Forward Attenuator	——	——	——	——
AC Amplifier	——	——	——	——
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Memory	——	——	——	——
Offset	——	——	——	——
Feedback Attenuator	——	——	——	——
(Deflection) Inverter	——	——	——	——
Vertical Amplifier	——	——	——	——
Dual-Trace Multivibrator	——	——	——	——
Vertical Output Amps	——	——	——	——

**=See sampling head
NSD = Nothing very similar described

1S1	1S2	3S1	3S2	3S3	3S5 3S6	3S76	4S1	4S2	4S2A	4S3
——	——	——	3S5	——	p82	——	——	——	——	——
p59	3S5	p79	3S5	NSD	p82	NSD	NSD	NSD	3S1	NSD
p58	——	——	**	——	**	NSD	NSD	——	——	NSD
——	3S1	p78	**	——	**	——	——	NSD	3S1	——
p58	S-1	p78	**	NSD	**	NSD	NSD	NSD	3S1	NSD
——	——	p79	3S1	——	——	——	——	——	——	——
p59	——	S-1	**	——	**	1S1	NSD	——	S-1	——
p60	S-1	1S1	——	1S1	——	1S1	1S1	1S1	S-1	1S1
——	S-1	S-1	**	——	**	——	——	——	S-1	——
p61	S-1	S-1	**	NSD	**	NSD	NSD	NSD	NSD	NSD
p61	1S1	1S1	1S1	NSD	p86	NSD	1S1	1S1	1S1	1S1
p62	1S1	1S1	3S5	1S1	p86	NSD	NSD	NSD	NSD	NSD
p66	3S5	3S5	3S5	1S1	p90	1S1	1S1	1S1	1S1	1S1
p66	3S5	3S5	3S5	1S1	p90	NSD	1S1	1S1	1S1	1S1
p68	p72	1S1	1S1	1S1	p94	1S1	NSD	NSD	NSD	NSD
p68	p72	1S1	1S1	NSD	p87	1S1	1S1	1S1	1S1	1S1
——	——	3S5	3S5	NSD	p91	NSD	NSD	NSD	NSD	NSD
p67	p73	3S5	3S5	NSD	p98	NSD	NSD	NSD	NSD	NSD
——	——	3S5	3S5	NSD	p102	NSD	NSD	NSD	NSD	NSD
——	——	3S5	3S5	3S5	p103	NSD	NSD	NSD	NSD	NSD

INDEX TO CIRCUIT DESCRIPTIONS: TRIGGERING and TIME BASE CIRCUITS

CIRCUITS	1S1	1S2
± Slope Selector	p118	p131
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Staircase Attenuator	p161	p172
Staircase Inverter	p161	p172
Timing Ramp Comparator	p161	1S1
Sampling Command Pulse Generator	p161	1S1
TDR-Pulse Delay	——	p172
Staircase (or Sweep Ramp) Gating	p161	p176
Step Driver	p167	——
Staircase (or Sweep Ramp) Generator	p168	p176
Horizontal Output Amplifier	——	——

NSD= Nothing very similar described

3T2	3T4	3T6	3T77A	5T1A	5T3
p137	1S1	p144	p154	NSD	NSD
p137	1S1	p144	p154	1S1	NSD
1S1	1S1	p146	1S1	NSD	NSD
p137	1S1	p144	p154	NSD	NSD
p138	NSD	p148	p155	NSD	1S1
——	——	p149	——	——	——
p208	1S1	p180	p196	3T77A	1S1
p206	NSD	p182	p197	3T77A	1S1
p206	1S1	p182	p197	3T77A	1S1
3T5	1S1	p181	p197	3T77A	1S1
p208	1S1	p181	p197	NSD	1S1
——	——	——	——	——	——
3T5	3T77A	p190	p200	3T77A	3T77A
1S1	NSD	p190	p200	3T77A	1S1
3T5	1S1	p193	p201	3T77A	NSD
p225	NSD	p193	NSD	NSD	NSD

SAMPLING SCOPE VERTICAL CHANNEL CALIBRATION

CALIBRATION ADJUSTMENTS		1S1	1S2	3S2	3S5 3S6	S-1	S-2
Variable Gain Bal		R168*	R388	—	—	—	—
Position Range Centering		R194	R396	R766	R472*	—	—
Memory Amp Bal	Ch A	R110	R247	R247	R167	—	—
	Ch B	—	—	R547	R367	—	—
Sampling Gate Volts	Ch A	R22	R367•	**	**	R26	R26•
	Ch B	—	—	**	**	—	—
Avalanche Volts		—	R131	**	**	R66	R66
Snap-off Current		R85	R140	**	**	R57	R57
Blowby Compensation	Ch A	—	R129	**	**	R13	C13 ■
	Ch B	—	—	**	**	—	—
(Strobe) Delay	Ch A	—	—	R60	R461	—	—
Offset Zero	Ch A	—	—	—	R649	—	—
	Ch B	—	—	—	R749	—	—
Sampling Gate Bal	Ch A	R30	R360	**	**	R22	R22
Low Noise	Ch A	—	—	—	—	—	—
	Ch B	—	—	**	**	—	—
Low Noise	Ch B	—	—	—	—	—	—
Inverter Zero	Ch A	—	—	—	—	—	—
	Ch B	—	—	—	—	—	—
(Feedback) Atten Zero	Ch A	—	—	—	R86	—	—
	Ch B	—	—	—	R286	—	—
Mem Gating Pulse	Ch A	R95	R204	R80	R580	—	—
Width	Ch B	—	—	R50	R550	—	—
Sampling Loop Gain	Ch A	C135	R168	C276	C184	R46	R46
	Ch B	—	—	C257	C384	—	—
Max Forward Gain	Ch A	—	—	—	R55	—	—
	Ch B	—	—	—	R255	—	—
Standard Gain (+ down)	Ch A	—	—	—	—	—	—
(+ up)	Ch A	—	R356	R301	R404	—	—
(+ down)	Ch B	—	—	—	—	—	—
(+ up)	Ch B	—	—	R601	R424	—	—
Volts per Div	Ch A	R172*	R317*	R764*	R470*	—	—
	Ch B	—	—	—	—	—	—
Rho per Div	Small Step	—	R353	—	—	—	—
	Large Step	—	R351	—	—	—	—
A-B (Added) Bal		—	—	R756	R430	—	—
Offset Cal	Ch A	—	—	—	R638	—	—
	Ch B	—	—	—	R738	—	—

* Front Panel Screwdriver Adjustment
** In Sampling Head
• Absent for Some Serial Number Ranges
■ R13 for Early Serial Number

S-3	S-4	3S1	3S3	3S76	4S1	4S2	4S2A	4S3
—	—	—	—	—	—	—	—	—
—	—	R766	R661	—	—	—	—	—
— —	— —	R247 R547	R335 R335	R1136 R2136	R1125 R1125	R1125 R1125	R1125 R1125	R1125 R1125
R26 —	— —	R198 R498	R169 —	R1057 R2057	R1067 R2067	R1074 R2074	R1023 R2023	R1045 R2045
R66	R66	R5	—	—	—	R1057	R1054	—
R57	R57	R76	R205	R2012	R2007	—	R1063	R1067
—	R18	C130 C131 C133	—	—	—	—	C1010	—
—	—	C430 C431 C433	—	—	—	—	C2010	—
—	—	—	—	—	—	—	—	—
— —	— —	— —	— —	— —	— —	— —	— —	— —
R22 — — —	R32 — — —	R192 — R492 —	R175 R185 R235 R245	R1063 — R2063 —	R1063 — R2063 —	R1078 — R2078 —	R1027 — R2027 —	R1050 R1056 R2050 R2056
— —	— —	R283 R583	R421 R441	— —	R1161 R2161	R1161 R2161	R1161 R2161	R1161 R2161
— —	— —	— —	— —	— —	— —	— —	— —	— —
— —	— —	R52 —	R215 —	R2023 —	R2022 —	R2045 —	R1067 —	R2073 —
R46 —	R49 —	R212 R512	R313 R313	R1088 R2088	C1107 C2107	C1107 C2107	C1107 C2107	C1107 C2107
— —	— —	— —	— —	— —	— —	— —	— —	— —
— — — —	— — — —	— R301 — R601	 R354 — R414	R1172 R1161 R2172 R2161	— — — —	— — — —	— — — —	— — — —
— —	— —	R756 —	R439* R459*	— —	R1172* R2182	R1172* R2182	R1172* R2182	R1172* R2182
— —	— —	— —	— —	— —	— —	— —	— —	— —
—	—	R764*	—	R1209*	—	—	—	—
— —	— —	— —	— —	— —	— —	— —	— —	— —

SAMPLING SCOPE TRIGGER AND TIME BASE CALIBRATION

CALIBRATION ADJUSTMENTS	1S1	1S2	3T2	3T4	3T5 & 3T6	3T77 & 3T77A	5T1 & 5T1A	5T3
TRIGGERING ADJUSTMENTS								
DC-Coupled Input Zero	—	—	—	—	R24	—	—	R103
Control-TD Bias	R460	R544	R82	—	R162	R44	R65	R210
2nd Recognition TD Bias	—	—	—	—	R112	R24	—	—
Arming TD Bias	—	—	—	—	R100	—	R35/R55	—
1st Recognition TD Bias	R420	R523	R72	R16	R36	R21	R25/R45	R172
UHF Sync Sensitivity	—	R481	—	—	—	—	—	—
Auto Trig Level	—	—	—	—	R32	—	—	—
±Trig Level Zero	—	—	—	—	—	—	—	R120
Minimum Holdoff Time	—	—	—	—	—	—	C146	—
SLEWING START ADJUSTMENTS								
Staircase Start Level	R270	R753	—	R263	—	R181	R381	R585
Timing Ramp Comparator Sens	R320	R677	—	R130	—	R94	R273	R345
Staircase Inverter DC Zero	R380	R681	—	R70	—	R63	R225	R376
Staircase Atten DC Zero	—	—	—	R60	—	—	—	—
Time Position (Delay) Zero	R370	—	—	R99	R591	R58	R220	R390
2nd Delay Zero	—	—	—	—	R574	—	—	—
Timing Ramp Start Linearity	—	—	—	—	—	—	R254	—
TIME BASE ADJUSTMENTS								
Horizontal Gain	**	**	R785*	R356*	R736*	R356*	—	—
Sweep Length	R290	R787	—	R245	—	R145	R345	R612
Position Centering	—	—	—	R341	—	R341	—	—
Real-Time Clock Frequency	—	—	—	—	L145	—	—	L625
Real-Time Sweep Cal	—	—	—	—	—	—	—	R515
Timing Ramp Slope Slowest	R335	R588	R336	R110	R518	R85	R267	R340
Next	—	—	—	—	—	R79A	—	—
Next	—	—	—	—	—	R79B	—	—
Fastest	C325	C585B	C329	C124	C539	C88G	C260F	C343
2nd Fastest	—	—	—	—	—	C88E	—	C350H
Dots Per Time/Div 10	—	—	—	C258A	—	C156	***	***
100	—	—	C452	C258C	R676	C158	***	***
DELAY ADJUSTMENTS								
Digital Clock Frequency	—	—	—	—	L145	—	—	—
Digital Clock Stability	—	—	—	—	R158	—	—	—
Digital Clock Start	—	—	—	—	R121	—	—	—
Analog Delay Cal	—	R661	—	R85	—	—	—	—
Programmed Analog Delay Cal	—	—	—	R80	—	—	—	—
1-Kilometer TDR Pulse Start	—	R621	—	—	—	—	—	—
100-Meter TDR Pulse Start	—	C615F	—	—	—	—	—	—
10-Meter TDR Pulse Start	—	C615H	—	—	—	—	—	—
RANDOM MODE ADJUSTMENTS								
Horizontal Output Zero	—	—	R516	—	—	—	—	—
Servo-Loop Bal	—	—	R536	—	—	—	—	—
Timing-Ramp Amplifier Gain	—	—	R348	—	—	—	—	—
Timing-Ramp Amplifier DC Zero	—	—	R376	—	—	—	—	—
Time Position Zero	—	—	R364	—	—	—	—	—
Slewing Ramp Slope All	—	—	R269	—	—	—	—	—
Fastest	—	—	C265	—	—	—	—	—
Leadtime	—	—	R231	—	—	—	—	—
1-ms (Rate Level) Correction	—	—	R622	—	—	—	—	—

* Front-Panel Screwdriver Adjustment
** Mainframe Front-Panel Adjustment
*** Dots Per Div Adjustment Not Needed

NOTES

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